Click model number for photo

2551 SCALER/COUNTER

4434 LATCHING SCALER

4448 COINCIDENCE REGISTER/LATCH

- CAMAC Packaging
- NIM, TTL, and ECL Level Compatibility
- High Data Rate for Fast Counting
- High Capacity and Density
- Control Via CAMAC or External Signals

COUNTING AND REGISTRATION OF LOGIC PULSES

Scalers and latches are data acquisition units that register logic pulses received during a given period. These logic pulses are often generated by discriminators whose function is to output a pulse when an analog signal exceeds a given threshold or level of interest. However, scalers and latches can also be used with other logic modules, including coincidence units, to count or register the number of simultaneous pulses.

Scalers such as the Model 2551 and the Model 4434 count the input signals during an active period. Latches, on the other hand, are data acquisition units that record logic levels ("hit patterns") in coincidence with a gate pulse. The Model 4448 Coincidence Register is a latch with 48 inputs and can be used in fast trigger applications.

FEATURES

Conforms to CAMAC Standards - Each of the three units is packaged in single-width CAMAC (IEEE-583) modules which offer the highest level of versatility and flexibility in configuring a system while fulfilling the requirements of the specific application.

High Counting Rate - The scalers are designed for high counting rate capability to limit data loss. The

2551 exhibits 100 MHz counting rate while the 4434 has > 30MHz instantaneous rate.

Accepts Various Inputs - Input to the scalers can be at least one of three common logic pulse formats. This flexibility ensures compatibility with most data collection systems. The Model 2551 accepts NIM level inputs, the 4448 accepts ECL and the 4434 accepts ECL levels or TTL (factory option).

High Density - Each unit allows multiple inputs which reduces the physical size and cost of most setups. The Model 2551 has 12 inputs, the 4434 has 32 inputs and the 4448 has 48 separate inputs.

FUNCTIONAL DESCRIPTION

SCALERS AND COUNTERS

Both non-latching, Model 2551, and latching scalers, Model 4434, record the number of input pulses. However, latching scalers can internally store the number of counts for each channel in a buffer. This buffer is independent of the input and can be read out during data collection. In either case, the active duration of the scaler can be a fixed or variable interval depending on the actual application. For example, some applications require data to be collected for a preset time interval. In other cases, the scalers are disabled by Inhibit pulses when certain prede termined conditions are ascertained by associated equipment.

Model 2551- 12-Channel Scaler

The Model 2551 contains 12 identical 24-bit binary scalers especially designed for use in high speed counting applications. This high performance unit has a capacity of 16,777,215 counts in each of its 12 channels. Added flexibility is provided by allowing cascading of even channels into odd ones by the use of internal jumpers to produce a 48-bit count capacity for up to a total of six channels.

Each scaler is equipped with an extremely wideband input circuit which responds to NIM level logic signals of any duration down to 5 nsec, without multiple-pulsing (in case of wide inputs). The ability to recognize narrow input signals at an equivalent rate of > 100 MHz is an important feature, since it assures that the scaler will accurately accumulate any output signal generated by standard discriminator and logic circuits.

Each module is provided with a high-speed fast inhibit which permits simultaneous rejection of input signals at a rate equivalent to 100 MHz. The CAMAC Inhibit (I) provides remote inhibit control from the data acquisition system. The inhibit signal must overlap the input signal. Toggling the inhibit will not cause false pulses to be counted.

Fast rejection of unwanted data is provided by the clear input. This input causes every scaler to be reset by application of a NIM level clear pulse without the need to perform any dataway operations.

The 2551 has a built-in test circuit which allows all channels to be checked. Application of the CAMAC Increment F(25) Function Code causes each scaler to advance by one count. The test circuit may be used without discon necting cables if the CAMAC Inhibit is on. Individual channel non-destructive readout is accomplished by generat ing a CAMAC Read F(0) and the appropriate address. Using Read and Clear

F(2), the channels will be automati cally zeroed after reading the last channel. Clear F(9), CAMAC Clear C, or Initialize Z will zero all channels.

Model 2551 Timing Diagram

Model 4434 - 32-Channel Latching Scaler

The Model 4434 contains 32 channels of 24-bit scalers in a single-width CAMAC module. Through the extensive use of LeCroy custom built hybrid circuits, the 4434 achieves a dramatic increase in channel density with a very low overall cost per channel.

Signal inputs to the 4434 are complementary ECL levels compatible with ECLine modules. Single-ended TTL levels are available as a factory option. Each scaler counts logical signals which have a duration of > 10 nsec and a maximum frequency of 20 MHz. The maximum instantaneous rate for the scaler is 30 MHz and a local double pulse resolution of 30 nsec is permitted.

Each channel in the module is followed by an internal buffer (latch) which may be used to store and readout accumulated data during subsequent counting. This readout may take place at any time under standard CAMAC control or under an independent Auxiliary Data Bus control via the front-panel 34-pin connector. In either case, the readout can be performed sequentially or randomly.

LOAD, CLEAR and VETO/INHIBIT input commands can be sent over the CAMAC DATAWAY or via Lemo connectors on the front panel. A common side switch selects NIM or TTL input levels and impedances for the connectors. Test, unit initialize and other commands are available from CAMAC only.

Receipt of a CAMAC or front-panel LOAD command temporarily halts all the scalers for approximately 220 nsec and transfers the contents to the internal buffer memory (see Timing Diagram). The scalers may then be optionally reset before counting is resumed with a CLEAR command. The duration of this action is approximately 100 nsec during which the module's inputs are disabled.

During data acquisition, unwanted data is rejected for the duration of a front-panel VETO signal or CAMAC Inhibit command.

Model 4434 Timing Diagram

LATCHES

Model 4448 Coincidence Register

The Model 4448 Coincidence Register is a latch unit offering fast storage capability at an unprecedented high density and low cost. Its complementary ECLine receiver input stage, compatible with inexpensive twisted-pair cable, makes it perfectly suitable for both small and large multiwire proportional chamber and hodoscope systems. The three fast analog outputs, providing majority information, are extremely useful in fast trigger decision applications.

The logic channels, which seek a coincidence between each input and a common fast gate input, provide coincidence resolving times under 3 nsec. Logical "1" data levels, representing the time coincidence between the common gate and the 48 inputs, are stored in three 16-bit buffer register groups for later

readout under CAMAC commands. The facility of performing majority logic is provided by three front-panel summing outputs which are each driven by 16 logic channels. The output current of the summing circuit is proportional, in increments of 100 mV ±10% into 50 ohm per register bit, to the number of coincidences stored in the register.

A front-panel clear input allows NIM levels to clear all three register memories. However, if the clear signal is "True" during the gate input, the outputs of the register memory and analog sum correspond to the coincidence overlap. This feature permits this unit, in conjunction with a discriminator, to be used as a majority logic unit when its clear input is locked in the enabled state. In addition, clear for the three individual 16 input groups is provided via CAMAC.

Pattern information can help speed off-line data sorting and provide a mapping of zero-suppressed recorded data of the detector/sensors. The outputs of three Model 4413 discriminator modules, for example, could be latched into a single 4448. Large detectors arrays such as hodoscope or an MWPC could employ such a system since over 1100 inputs can be housed in a single CAMAC crate.

Model 4448 Timing Diagram

SPECIFICATIONS

Model 2551

INPUT

Signal Input: 12, all identical, > -600 mV NIM logic levels into 50 ohm; direct coupled; < 10% reflection typical at 1 nsec rise time; protection to ±5 V transients. Minimum pulse width 7 nsec FWHM at -600 mV input amplitude; 5 nsec FWHM at -700 mV input amplitude. Multiple pulse resolution is 10 nsec; counting rate is DC to 100 MHz.

Inhibit: Common input, -500 mV threshold, impedance 50 ohm, 5 nsec minimum width. Inhibit signal stretches internally by approximately 5 nsec and must precede input signal by 10 nsec. Inhibit pulses will not be counted by scaler.

Clear: Common input, -500 mV threshold, 50 nsec minimum width clears all channels within 1 µsec.

GENERAL

Capacity: 24 binary bits (16,777,216), or 48 bits by cascading channels.

Cascading of Channels: By internal wire jumper option, each even-numbered channel (i.e., 0, 2, 4, 6, 8, 10) may be cascaded with the subsequent odd-numbered channel to provide one 48-bit scaler. In this mode of operation, no LAM will be generated by either of the cascaded channels.

Half Scale Flag: Any scaler generates LAM when 24th bit is set.

Packaging: In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF-shielded CAMAC #1 module.

Power Requirements: 1.2 A at +6 V; 100 mA at -6 V.

Note: By internal wire jumper option, even numbered channels may be cascaded with subsequent odd numbered channels to provide 48-bit channels. Any scaler generates LAM when 24th bit is set.

Model 4434

INPUT

Signal Inputs: 32, in two 2 x 17 pin front-panel connectors. Differential ECL (TTL factory option); 110 ohm pin-to-pin with differential ECL, 560 ohm to ±5 V for TTL.

Minimum Input Pulse Width: 10 nsec. Double pulse resolution is < 30 nsec. Maximum frequency is > 20 MHz; maximum instantaneous rate is > 30 MHz.

LOAD, CLEAR and VETO Inputs: Each have a single front-panel Lemo-type connector; a common side-switch selects either negative going NIM or TTL levels, input impedance 50 ohm for NIM pulses; 50 ohm AC and 100 ohm DC to 5 V for TTL pulses.

Load Input: A load pulse (> 10 nsec width) will disable input for 220 nsec and shift the scaler contents into a 32 -word x 24-bit buffer; LOAD can optionally generate a LAM on the CAMAC dataway and also prepare the memory for readout by loading the starting subaddress (FA) and readout number (RN) previously defined by a CAMAC F(16) or Z; a front-panel LED (RDE, Readout Enabled) is lit in recognition of a Load signal.

Clear Input: A CLEAR pulse with > 20 nsec width will disable inputs for a duration of approximately 100 nsec and clears the 32 scalers.

Veto Input: Disables inputs for the duration of the VETO (action identical to CAMAC INHIBIT).
GENERAL

Packaging: Single-width CAMAC standard module.

Power Requirements: 3.1 A (ECL version) at +6 V; 2.8 A (TTL version) at +6 V; 400 mA (ECL version) at -6 V; 40 mA (TTL version) at -6 V.

OPTION SWITCHES

A set of side accessible switches allows the user to select different options as follows:

LAD: Latching Disable; when ON the module works as a normal non-latching scaler.

OVF: Overflow determines whether an overflow condition occurs when bit 16 of any scaler is ON or when bit 24 is ON.

LCO: Load and Clear at Overflow when ON.

LOF: LAM at Overflow; a LAM is generated when at least one channel reaches the overflow set value.

LRE: LAM at Readout Enable; a LAM is generated after a readout request.

LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there are data to be read.

BAD: 4-bit Bus Address; defines module address in the auxiliary bus.

VBR: Veto by Bus Readout; enables a veto of all scaler inputs during the loading of the auxiliary bus output registers (< 200 nsec).

NIM/TTL: Determines pulse standard accepted by inputs LOAD, CLEAR and VETO. NIM: 0 = 0 mA, 1 = -12 mA; TTL: 0 = +2.5 V, 1 = +0.5 V.

AUXILIARY BUS

A total of 16 LeCroy Model 4434 modules may be interfaced to an auxiliary bus via a front-panel 34-pin connec tor. The auxiliary bus must end in an independent dedicated controller. Use of the auxiliary bus permits addressed readout of the scaler contents independent of CAMAC operations for applications such as raster scan display.

Model 4448

INPUT

Signal Inputs: 48, all identical. Differential ECL, 100 ohm direct coupled; < 10% at 2 nsec rise time. Minimum width 4 nsec. Input sensitivity ±20 mV.

Double Pulse Resolution: 8 nsec maximum, 6 nsec typical.

Gate Input: One; Lemo-type connector; 50 W impedance; -600 mV or greater; minimum duration at full logic level (-750 mV), 3.0 nsec.

Clear Input: One; Lemo-type connector; -600 mV or greater, 50 ohm impedance; minimum duration 5 nsec, 2 nsec settling time after clear.

OUTPUT

Summing Outputs: 3 identical; one for each of the three groups A, B, C of 16 bits each; -100 mV ±5% into 50 ohm is presented for each register latched in the corresponding group of 16. Maximum output into 50 ohm, -0.7 V corresponds to 7 set registers; rise time 3 nsec, delay of leading edge of summing output from leading edge of coincident input is 9 nsec.

GENERAL

Gate-Input Delay: 2.5 nsec typical.

Coincidence Width: 2.5 nsec and up, determined by input and gate pulse durations.

Packaging: CAMAC single-width module.

Power Requirements: 400 mA at +6 V; 1.9 A at -6 V.

CAMAC COMMANDS

Model 2551 - 12-Channel Scaler

CAMAC COMMANDS

C or Z: All scalers and LAM are cleared by the CAMAC "Clear" or "Initialize" command. Z also disables LAM.

I: All Scaler inputs are inhibited during CAMAC "Inhibit" command.

Q: A Q = 1 response is generated in recognition of an F(0) or F(2) Read function, or an F(8) if LAM is set. There will be no response (Q = 0) under any other condition.

X: An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated.

L: A Look-At-Me signal is generated from the time when first 24th bit is set until a module Clear command. LAMs can be enabled or disabled and can be tested by Test LAM.

CAMAC FUNCTION CODES

F(0)·A(0-11): Read registers; 0 through 11.

F(2)·A(0-11): Read registers and Clear module and LAM; requires N and A (Clears on A(11) only).

F(8): Test Look-At-Me; independent of LAM disable. Q response is generated if LAM is set.

F(9): Clear all scaler channels simultaneously.

F(24): Disable Look-At-Me.

F(25): Increment all scalers. Inhibit should be True to prevent input pulses from being counted.

F(26): Enable Look-At-Me. Remains enabled until Z or F(24). Caution: The state of the LAM enable will be arbitrary after power turn-on.

Model 4434 - 32-Channel Latching Scaler

CAMAC COMMANDS

Z: Initialize the unit. All scalers, the buffer, LAM and register CR are cleared.

C: Clear all scalers.

I: All scaler inputs are inhibited during CAMAC INHIBIT command; the action is identical to that of the front-panel VETO input.

X: A X = 1 response is generated in recognition of any valid function.

Q: A Q = 1 response is generated in recognition of any executable function.

L: Look-At-Me signal can be generated according to several possible options.

CAMAC FUNCTION CODES

F(0)·A(0): Generates readout of the selected channel; F(0) can be executed and a Q = 1 response will be provided under the following conditions: a) Side switch LAD (Latching Disable) = ON; always if the LED RDE (Readout Enable) is ON b) Side switch LAD = OFF; only after a LOAD has been received and as long as the readout has not been completed.

F(2)·A(0): Sequential data readout with auto-increment of the address; F(2) can be executed and a Q = 1 re sponse will be provided independent of the Latch Disable switch position if a LOAD has been received, and as long as the readout has not yet been completed.

Note: if the number of scalers to be read is RN+1>32-FA then the readout (Where RN=Resolution and FA=First Address, after address 31) will continue with addresses 0, 1, 2, etc., until RN+1 channels have been read.

F(8)·A(0): Test LAM, Q = 1 response is generated when LAM is ON.

F(10)·A(0): Test and Clear LAM; a Q = 1 response is generated when LAM is ON. LAM is cleared at S2.

Note: LAM goes on again after F(10) in the following cases:

a) Switch LOF (LAM at Overflow) = ON and scaler not cleared.

b) Switch LDR (LAM Data Ready) = ON and data readout not finished.

F(16)·A(0): Load register CR (Command Register); F(16) can always be executed and a Q = 1 response is generated.

The Command Register is a 16-bit word with the following format and explanation:

Click here

FA: First Address to be read.

RN: Readout Number; defines how many channels (minus one) have to be read starting from the address FA; after a Z command, RN is set to 31 and FA to 0.

T: Test; T = 1 inhibits signal inputs; increments all scalers by one count; after a Z command T = 0.

LD: Load; LD = 1 performs a load if switch LAD (Latching Disable) = OFF; after 0.8 µsec the module will be ready for readout; enables functions F(0) and F(2).

CL: Clear; CL = 1 clears all the 32 scalers.

RD: Readout Enable; RD = 1 prepares the module for readout, does not require a LOAD; readout can be started after 0.8µsec.

BD: Bus Disable; BD = 1 disables the Auxiliary Bus readout; after a Z command BD = 0.

Model 4448 - 48-Input Coincidence Register/Latch

CAMAC COMMANDS

Z or C: Clears registers during S2. (Used for special test feature option.)

I: Inhibit gate input.

L: LAM: logic OR of all registers (switchable on or off for each register A, B, or C).

CAMAC FUNCTION CODES

F(0)·A(0): Reads register A (Inputs 1-16).

F(0)·A(1): Reads register B (Inputs 17-32).

F(0)·A(2): Reads register C (Inputs 33-48).

F(2)·A(0): Reads and clears register A.

F(2)·A(1): Reads and clears register B.

F(2)·A(2): Reads and clears register C.

F(8): Test LAM.

F(9)·A(0): Clears register A.

F(9)·A(1): Clears register B.

F(9)·A(2): Clears register C.

F(11): Clears all registers.

SCALER SELECTION CHART

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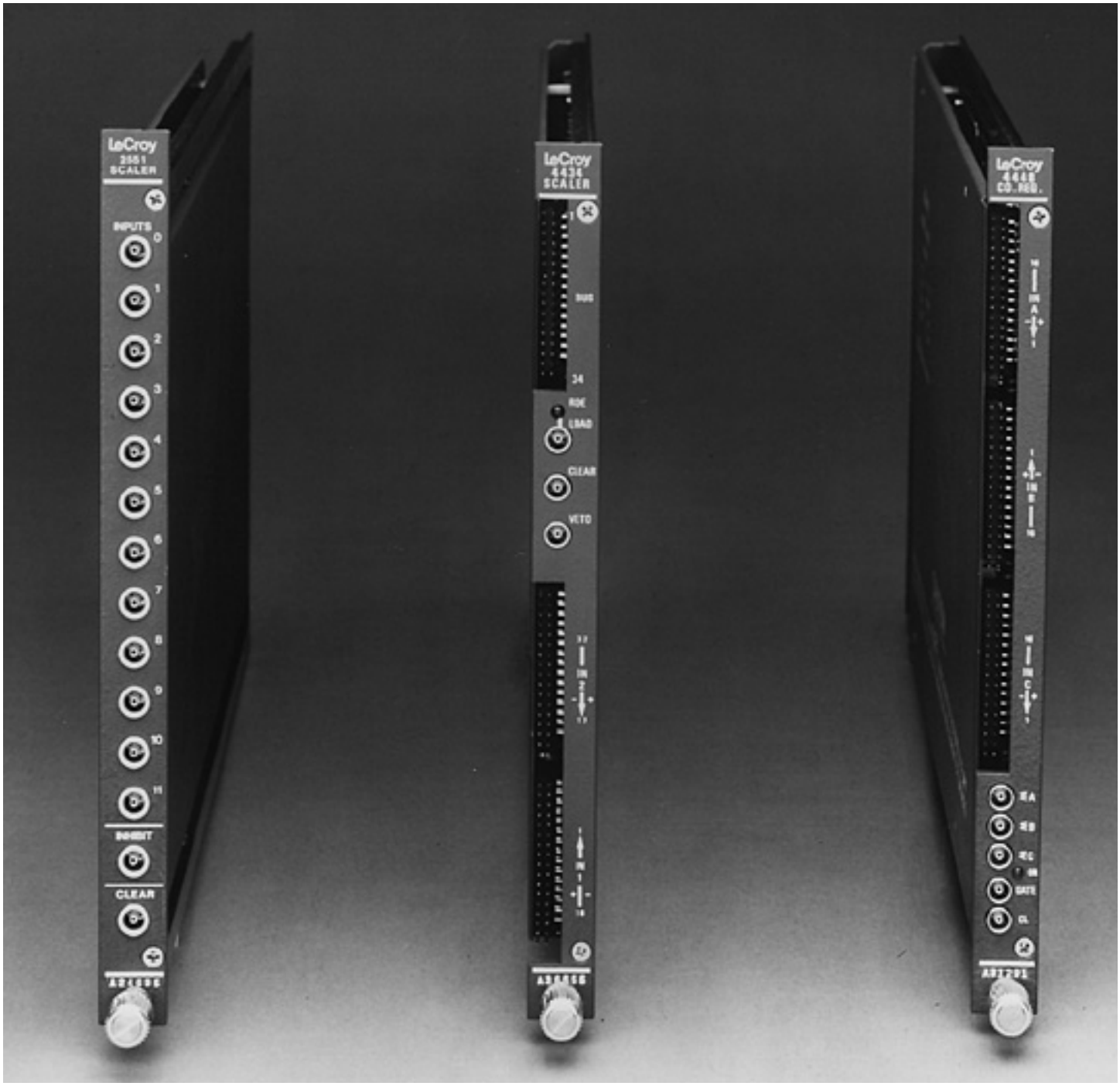
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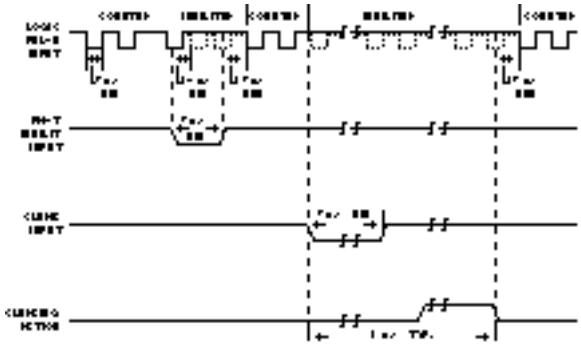

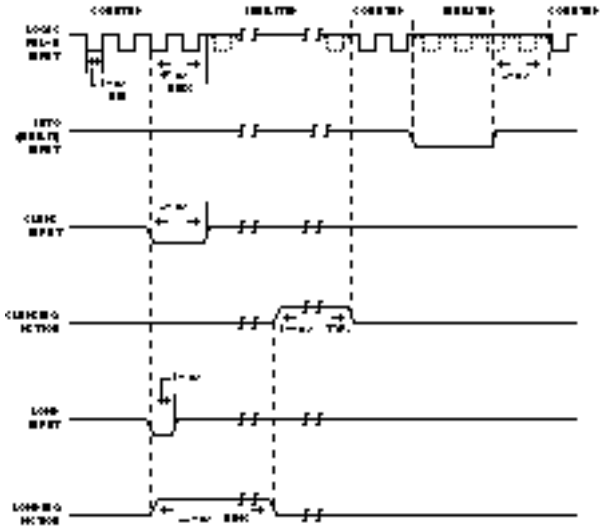

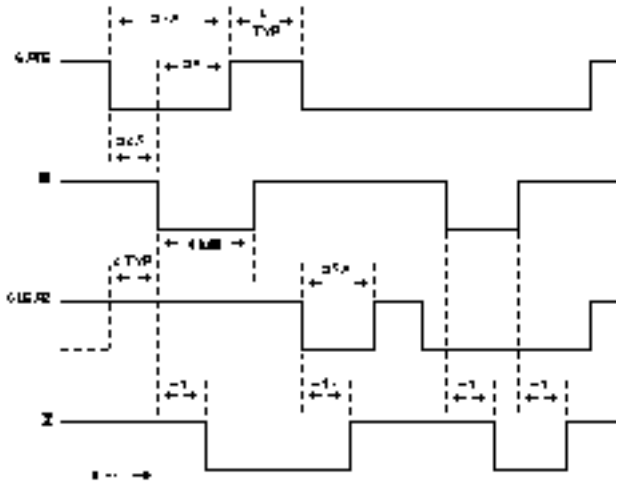

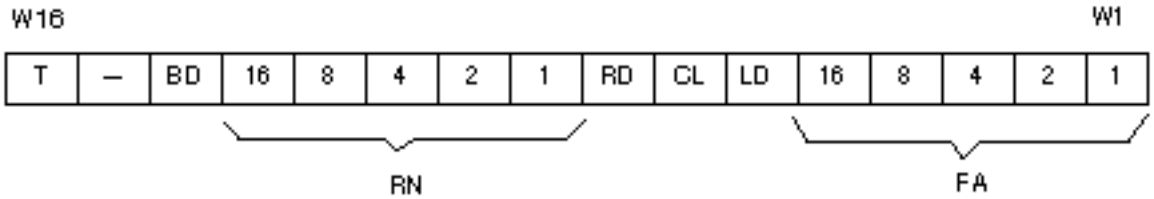
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Model	2551	4434	4448
GENERAL			
Function	Counter	Latching Counter	Latch
No. of Inputs	12	32	48
Rate (MHz)	100	20 typical, 30 instantaneous	150 MHz typical
Capacity	24 bits or 48 bits by cascading channels	24 bits (16,777,215 counts)	Ñ
Double Pulse Resolution	10 nsec	< 30 nsec	8 nsec max., 6 nsec typical
INPUTS			
Signal	NIM into 50 ohm	Differential ECL (TTL factory option)	Differential ECL
Clear	NIM -500 mV, ³ 50 nsec clears all channels within 1 µsec or via CAMAC command	NIM (TTL) > 20 nsec, will disable inputs for 100 nsec and clear scalers or via CAMAC command	2 nsec settling time after command, -600 mV, > 5 nsec
Inhibit/Veto/Gate	> 5 nsec must precede input by 10 nsec or via CAMAC inhibit, -500 mV	NIM (TTL) pulse or via CAMAC inhibit must completely overlap inputs	NIM -600 mV, > 3 nsec or via CAMAC inhibit
OUTPUTS			
Data Output	Via CAMAC	Via CAMAC or via auxiliary bus	Via CAMAC
Miscellaneous Output	n/a	Total of 16 4434s may be integrated to auxiliary bus.	3 summing outputs from each 16 input group. -100 mV ±10% presented for each register latched.
POWER CONSUMPTION			
+6 V	1.2 A	3.1 A (ECL version) 2.8 A (TTL version)	400 mA
-6 V	100 mA	400 mA (ECL version) 40 mA (TTL version)	1.9 A