Phillips Scientific

16 Channel Peak ADC

FEATURES

* The Model 7164 has LEMO Inputs
* The Model 7164H has Differential Header Inputs
* Less Than 7.2 µSec Conversion and Processing Time
* 12-Bit Dynamic Range, Resolution to 1 mV/Count
* Accepts Unipolar and Bipolar Input Pulse Shapes
* Programmable Pedestal Correction
* Sparse Data Scan with Lower and Upper Threshold Cuts
* Fast CLEAR and Common GATE Window
* Built-in Test Features Check ADC and Digitization

DESCRIPTION

The Model 7164 PEAK ADC implements 16 channels of Peak Detect and ' old followed by a digital processing section and CAMAC interface in a single width C/ | AC module. To minimize data readout time, the ADC performs a sparse data fun(|)n. Channels can be individually programmed with pedestal correction and both lowe nd upper level thresholds. Digitization starts following release of the Common | TE input. It may be delayed by a user-programmable amount to allow time for deriv | 'on of fast CLEAR signals before digitization starts.

Channels that meet the sparsification requirements will have corresponding ; its set in the Hit Register. Subsequent events will be ignored until the Hit Regis1 | is cleared either by completing a sparse read of the module or via front panel ; 1st CLEAR or CAMAC Clear commands.

ANALOG INPUTS

Unless otherwise noted, specifications are for single-ended 4.096 Volts full ; 1 ale and 50 ohm input impedance. Consult factory for available optional ranges (; to ±10V full scale and input impedance up to 1K ohm.

Voltage Compliance : ±20mV to ±4.096 Volts; Either positive, negative o, 'ue differential; (Specify when ordering).

Signal Shape : Any typical pulse shapes encountered in nu ; ?ar physics: Unipolar, Bipolar or Tripolar. Risetimes ∨ | 'hin the range of 50nSec to 50µSec.

Input Impedance
Single Ended : 51 ohm ±2%, direct coupled.
Differential : 102 ohm ±2%, direct coupled.

Dynamic Range : 4.096V full scale, 1mV/Count. ±2%, 12-bit Range.

Input Offset : 0 to 2mV, (40µAmp) maximum; (20µAmp Differenti: |

Slew Rate : 80Volt/µSec.

Stability Gain & Pedestal : Better than 100µV/°C between 0°C to 60°C.

Droop : Less than 50µV/µSec.

CLEAR, GATE and TEST INPUTS

LEMO Inputs (7164) : NIM logic levels; 2 connectors per input to facil te daisy chaining. Input impedance 5.1K ohm; 50 ohm terminate the last n dule in chain.

ECL Inputs (7164H) : Differential ECL logic levels; 2 pairs per input to facilitate daisy chaining; terminate at end of chain with 110 ohm.

Common GATE Input : Common to all channels; 50nSec to 50µSec; s uld precede the voltage peak by 20nSec minimum; no dependence on pos on of analog event within gate. Processing of events begins at end of GATE p se.

CLEAR Input : Common to all channels, accepts 10nSec or greate nput width.

Clear Settling Time : Less than 850nSec to within one count.

Clear Function : Timing assumes no conversion delay, causing di ization to start typically 600nSec after trailing edge of GATE.
(End of Gate – 700nSec) < t_{CLR} < Start of digiti tion: Resets front ends, aborts digitization cycle.
t_{CLR} **> Start of digitization:** No effect on front ends digitization.

TEST Input : Leading edge causes a GATE and analog input to applied to all channels. Digitizes to approximately 1/4 full scale calibratior NOT intended for precise calibration of the module.

BUSY Output

LEMO (7164) : Two paralleled LEMO connectors; Double-amplitude egative NIM logic 32mA.

ECL (7164H) : Two pairs of double row pins; Differential ECL logic vels.

Active from the trailing edge of common GATE until the Hit Register s been cleared, explicitly by either the front panel CLEAR input or by one of the CAMAC clear mmands, or implicitly by completion of a sparse read function. The CLEAR input signal caus ; BUSY to go active for 750nSec. The module will not recognize a new GATE while BUSY is activ

FRONT END PERFORMANCE

Linearity

Integral : Less than 3 counts over 10% to 90% of range.
Differential : Dithering disabled: Less than ±0.5LSB from 0 to 4)5 counts.
6-bit dithering: Less than ±0.06LSB from 64 to 40. counts.
7-bit dithering: Less than ±0.025LSB from 128 to . '67 counts.

Crosstalk : 1 LSB maximum between adjacent channels opera l within range.

Conversion Time 7.2 µSec maximum; No conversion delay inserted.

Conversion Delay : Digitization begins 600nSec after trailing edge c GATE to allow time for settling and for accepting fast CLEAR signals. Digi ation may be delayed by 0 to 16µSec in 62.5nSec increments with extern jumpers. The increased delay may be used to allow a greater acceptance w low for CLEAR signals.

Power Supply Requirements :

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+ 6V    @  2.4 Amp typically
– 6V    @  1.8 Amp typically
+24V    @  510 mA typically
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Forced air cooling is recommended.

ADDITIONAL TEST FEATURES

Calibration Check : Simulates a Voltage/Gate sequence under CAMAC cont: | to verify operation of the module. CAMAC selectable nominal 1/20 or 1/4 fu | scale calibration. Not intended for precise calibration of the module.

CAMAC Check : Loads a predetermined pattern to simulate the outputs | f the A/D converters. Useful for verifying the operation of the processing sectic | ; of the module.

SPARSIFICATION and LAM OPERATION

Separate pedestals and upper and lower thresholds may be set for | ich channel. They are enabled using bits in the Control Register. Pedestals in signed 2's compl | ient format are added to the data before threshold comparison. Bits in the Hit Register are s | during digitization for those channels whose pedestal corrected data falls within their upper | d lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data | ids present only those channels with bits set in the Hit Register, starting with the highest number | ' channel. As channels are read, their Hit Register bits are reset. When the final channel has been | ad LAM is reset.

DATA WORD FORMAT

16	13	12	1
Channel ID		Channel Data	

CONTROL REGISTER FORMAT

| 16	9	8 4	3	2		1
Conversion Delay (Read Only)		0	UT Enable	LT Enable	PE	Enable

CAMAC DATAWAY OPERATIONS

F(0)·A(X) : Read event data memory for Channel (X+1). Data word as de | :ribed above.

F(1)·A(X) : Read the parameter memory pointed to by the most re(| it F17 operation for channel (X+1).

F(4)·A(0) : Read Sparse Data. Only those channels with data that falls | :tween the upper and lower thresholds are read, starting with the highest number | channel. Reading an empty buffer returns Q false. Data word as described above.

F(6)·A(0) : Read the Control Register. Format described above.

F(6)·A(1) : Read the Hit Register. Shows which channels' pedestal col | cted data falls within their upper and lower thresholds.

F(8) : Test LAM. A Q=1 response is generated if LAM is pres | it and enabled. The address lines have no effect on this command.

F(9) : Clear the Module. Resets front end, clears and disables L | 1, disables pedestals and thresholds. The address lines have no effect on this cor | 1and.

F(10) : Clear LAM. Occurs on S2 strobe. The address lines h | e no effect on this command.

F(11)·A(0) : Reset the Control Register. Occurs on S2 strobe.

F(11)·A(1) : Reset the Hit Register and LAM. No effect on data memory. | curs on S2 strobe.

CAMAC DATAWAY COMMANDS (continued)

F(11)·A(2) : Reset the Test Register. Occurs on S2 strobe.

F(11)·A(3) : Reset the Hit Register, LAM and data memory. Occurs S2 strobe.

F(16)·A(X) : Write to data memory for channel (X+1).

F(17)·A(0) : Select the Pedestal Memory for the next F1 or F20 ope tion.

F(17)·A(1) : Select the Lower Threshold Memory for the next F1 or '0 operation.

F(17)·A(2) : Select the Upper Threshold Memory for the next F1 or '0 operation.

F(17)·A(4) : Select the Test Register for the next F20 operation.

F(19)·A(0) : Set the Control Register bits. Format described above.

F(20)·A(X) : Write the pedestal, upper or lower threshold for Chann (X+1) as selected by the most recent F17 operation. Pedestal range is ±4095 hreshold ranges are 0 to 4095. Program the Test Register if it was selecte)y the most recent F17 operation.

$\qquad$ A0 : Test pattern = 001001001 1
$\qquad$ A1 : Test pattern = 010010010 0
$\qquad$ A2 : Test pattern = 100100100 0
$\qquad$ A3 : Test pattern = 111111111 1

F(23)·A(0) : Reset the Control Register bits. Format described abo

F(24) : Disable LAM. Occurs on the S2 strobe. The address l es have no effect on this command.

F(25)·A0 : Digital test. Initiates a data acquisition cycle using tl value stored in the Test Register by the most recent F20 command.

F(25)·A1 : Test. Initiates a data acquisition cycle using a simula d event of approximately 1/20 full scale applied to the front end.

F(25)·A2 : Test. Runs a data acquisition cycle using a simulated ent of approximately 1/4 full scale applied to the front end.

F(26) : Enable LAM. Enables LAM on the S1 strobe. The addr s lines have no effect on this command.

C, Z : Reset the front end, clear and disable the LAM, disab pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I : Inhibits peak detector front end.

(Front Panel Description)

PHILLIPS
7164
16 CHANNEL
PEAK ADC

CLEAR

GATE

BUSY
TEST
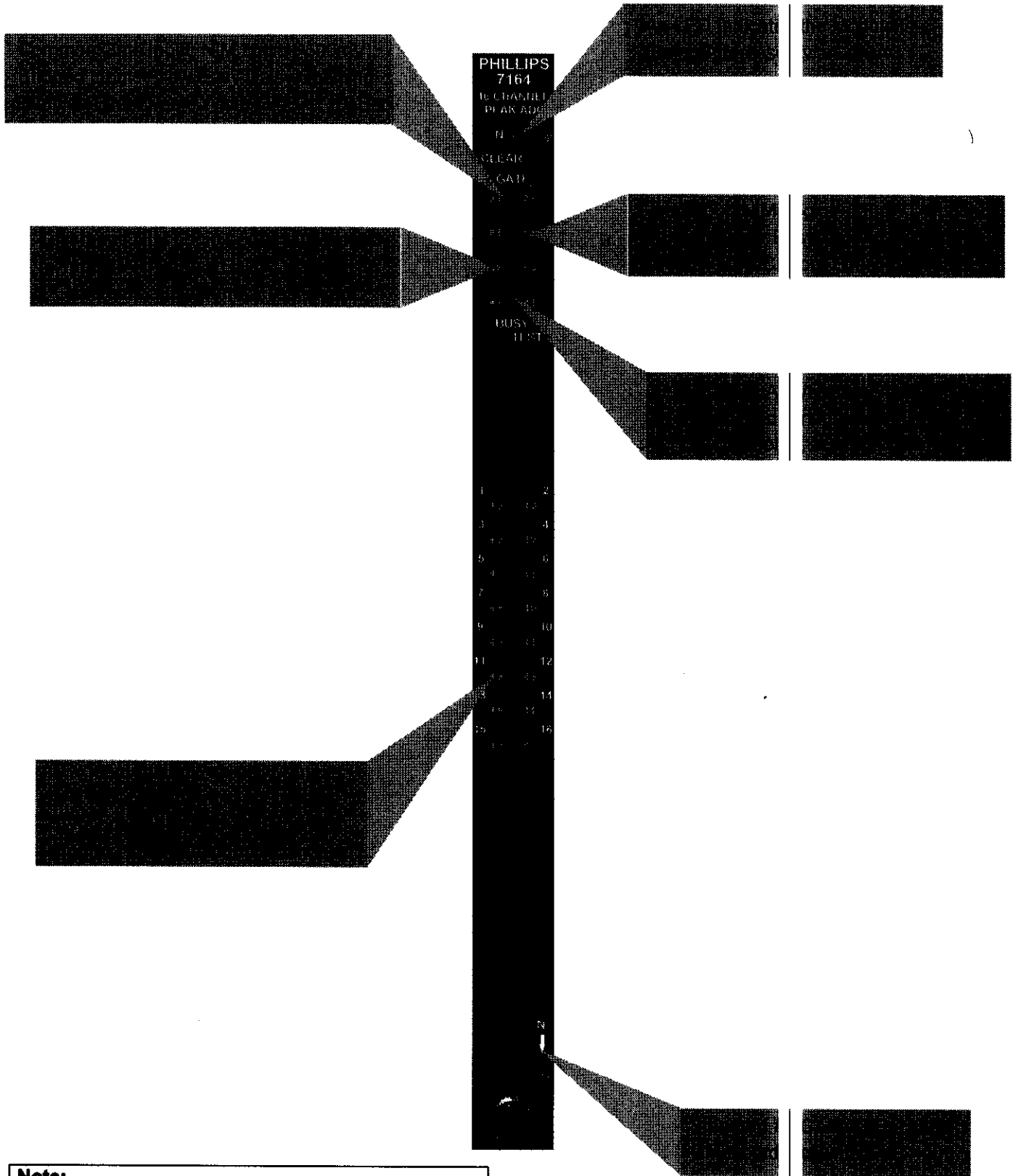
Note:

1). Rear Panel Jumper Provides a Programmable
    Conversion Delay of 16μSec in 62.5nS Increments.
    The Delay allows an Unwanted Event to be Cleared
    Before it is Digitized and Stored.

PROGRAMMING
MANUAL FOR

THE MODELS

7164 / 7164H

7166 / 7166H

7167 / 7167H

7186 / 7186H

7187 / 7187H

PROGRAMMING MANUAL FOR MODELS
7164/7164H,
7166/7166H, 7167/7167H,
7186/7186H, AND 7187/7187H

1. CAMAC DATAWAY OPERATIONS

1.1 Writing Data

F(16)›A(X): Write to data memory for channel (X+1).

1.2 Reading Data

F(0)›A(X): Read event data memory for Channel (X+1). Data wo l contains pedestal corrected data and the channel number. Data is present regardless c sparsification and is read non-destructively.

F(4)›A(0): Read Sparse Data. Only those channels with data that fal between the Upper and Lower Thresholds are read, starting with the highest numbered hannel. Each read presents the next channel on the hit list. As each channel is read, its bi 1 the Hit Register is reset. Reading an empty buffer returns Q false, X true.

16	13	12	1
Channel #		Channel Data	

Channel Data Format

1.3 Set the Control Register

F(19)›A(0)›D(X): Selectively enable the Pedestal, Upper and Low Thresholds for all channels.

    D1=1 Enable the Pedestals
    D2=1 Enable the Lower Thresholds
    D3=1 Enable the Upper Thresholds
    D4 to D15 = 1 No Action

1.4 Reset the Control Register

F(23)›A(0)›D(X): Selectively disable the Pedestal, Upper and Low Thresholds for all channels.

    D1=1 Disable the Pedestals
    D2=1 Disable the Lower Thresholds
    D3=1 Disable the Upper Thresholds
    D4 to D15 = 1 No Action

1.5 Read the Control Register

F(6)›A(0): Read the control register. This tells which of the Pedestal Jpper Threshold or Lower Threshold are enabled, as well as the programming of the Conve ion Delay.

16		9	8		4	3	2		1	
MSB	Delay Time	LSB		0		UT Enabled	LT Enabl		PED Enabled	

Control Register Data Format

1.6 Read the Hit Register

F(6)-A(1): Read the Hit Register. Shows which channels' pedestal co- | cted data fall within their Upper and Lower Thresholds. A 1 in any position indicates t | channel has passed sparsification. For example, 0100 0010 0000 1001 shows that data on | annels 1, 4, 10, and 15 have passed sparsification. These are the channels which will be | ad using the sparse data read function (F4).

16	1
Channel 16	Channel 1

Hit Register Data Format

1.7 Read and Write the Parameter Memory

Signed two's complement arithmetic is used. Pedestals occupy 13 | s giving a range of -4096 ($1000) to +4095 ($0FFF). Thresholds are 12 bits, ranging fron | to 4095.

1.7.1 Select the Parameter

F(17)-A(0): Select the Pedestal Memory for the next F1 or F2(| peration.

F(17)-A(1): Select the Lower Threshold Memory for the next | or F20 operation.

F(17)-A(2): Select the Upper Threshold Memory for the next | or F20 operation.

1.7.2 Write the Data

F(20)-A(X): Write the Pedestal, Upper or Lower Threshold | Channel (X+1) as selected by the most recent F17 operation.

1.7.3 Read the Data

F(1)-A(X): Read the Parameter Memory pointed to by | most recent F17 operation for channel (X+1).

1.8 Test Functions

1.8.1 Run a Test from the Test Registers

1.8.1.1 Select a Pattern

1.8.1.1.1 Select the Test Registers

F(17)-A(4): Select the Test Register for the | xt F20 operation.

1.8.1.1.2 Select a Pattern

F(20)-A(X): Program the Test Register if | was selected by the most recent F17 operation.

X	Pattern
0	001001001001
1	010010010010
2	100100100100
3	111111111111

1.8.1.2 Run A Test

F(25)-A0: Digital test. Initiates a data acquisition | cle using the value stored in the Test Register by the most recent F20 co | nand.

1.8.2 Run A Front End Full Scale Test

Models 7166/7166H, 7167/7167H, 7186/7186H and 7187/7187H

F(25)·A1: Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)·A2: Initiates a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

Model 7164/7164H

F(25)·A1: Initiates a data acquisition cycle using a simulated event of approximately 1/20 full scale applied to the front end.

F(25)·A2: Initiates a data acquisition cycle using a simulated event of approximately 1/4 full scale applied to the front end.

1.9 LAM

LAM is set during digitization when pedestal corrected data for at least one channel falls between that channel's Upper and Lower Thresholds.

F(24): Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(26): Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

F(8): Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(10): Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

1.10 Resets

F(9): Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(11)·A(0): Reset the Control Register. Occurs on S2 strobe.

F(11)·A(1): Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11)·A(2): Reset the Test Register. Occurs on S2 strobe.

F(11)·A(3): Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.

2. CAMAC NON-DATAWAY COMMANDS

C, Z: Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I: Inhibits front end functions.

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PROGRM.MAN 01/23/97

APPENDIX A

7164 / 7164H

PROGRAMMING

JUMPERS

7164 REAR JUMPER PROGRAMMING

CONVERSION DELAY TIME MULTIPLIER

(*62.5 nsec)

128
64
32
16   625 nsec SHOWN
8
4
2
1
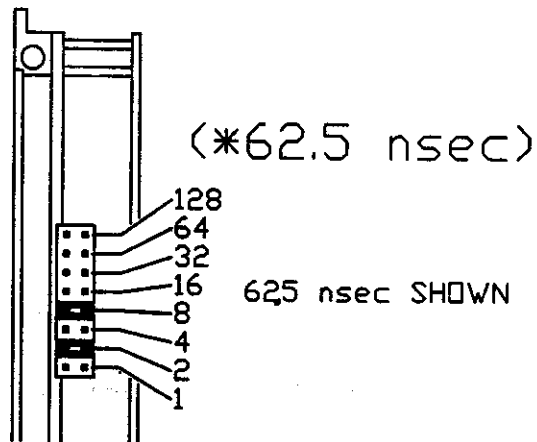
VIEWED FROM TOP REAR OF MODULE

7164 GATTI JUMPER LOCATION
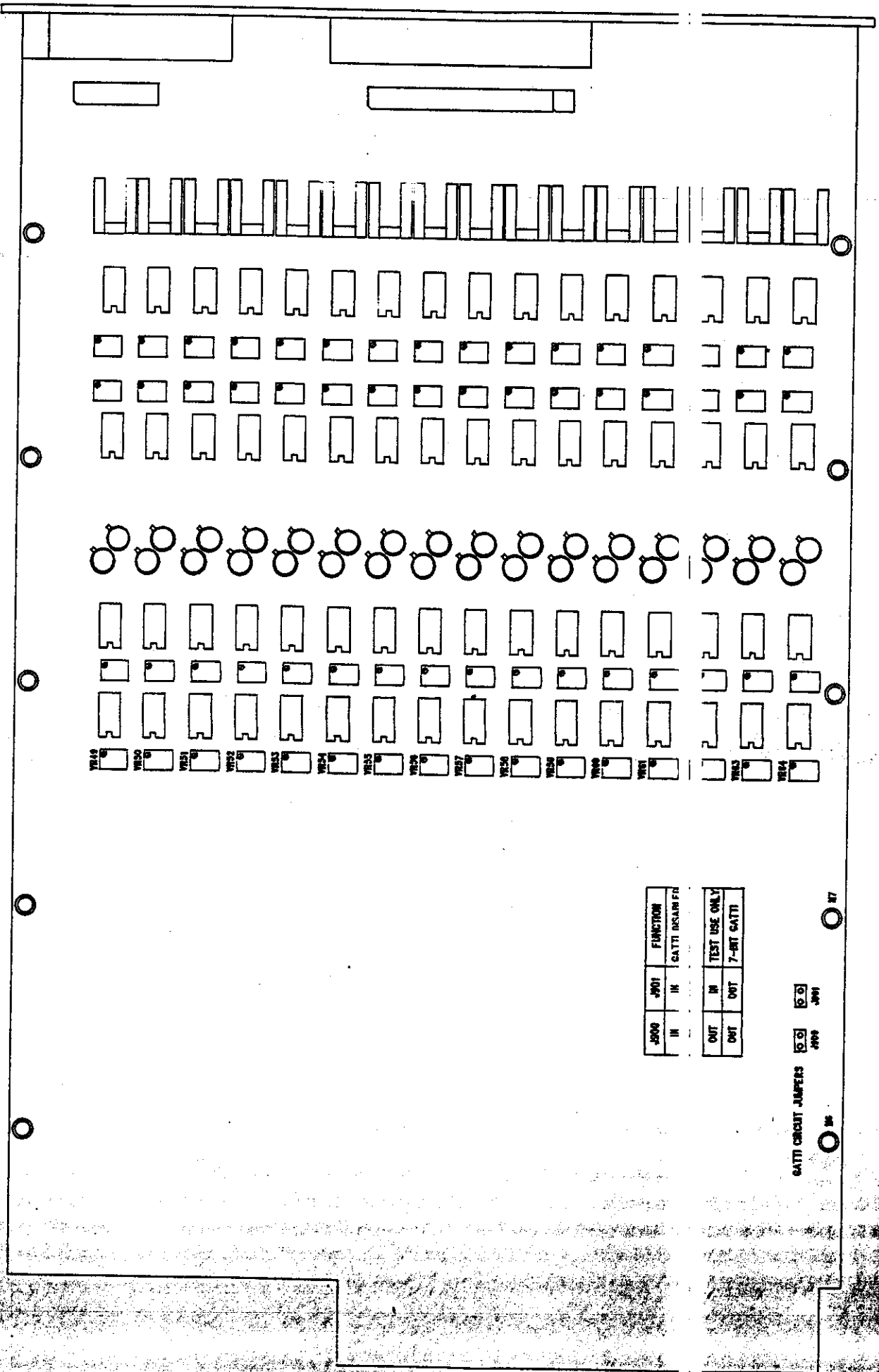
	J900	JI01	FUNCTION
	IN	IN	GATTI DISAM FR
	OUT	IN	TEST USE ONLY
	OUT	OUT	7-BIT GATTI

GATTI CIRCUIT JUMPERS

PHILLIPS SCIENTIFIC Test Program 5/20/1996 11:15:27
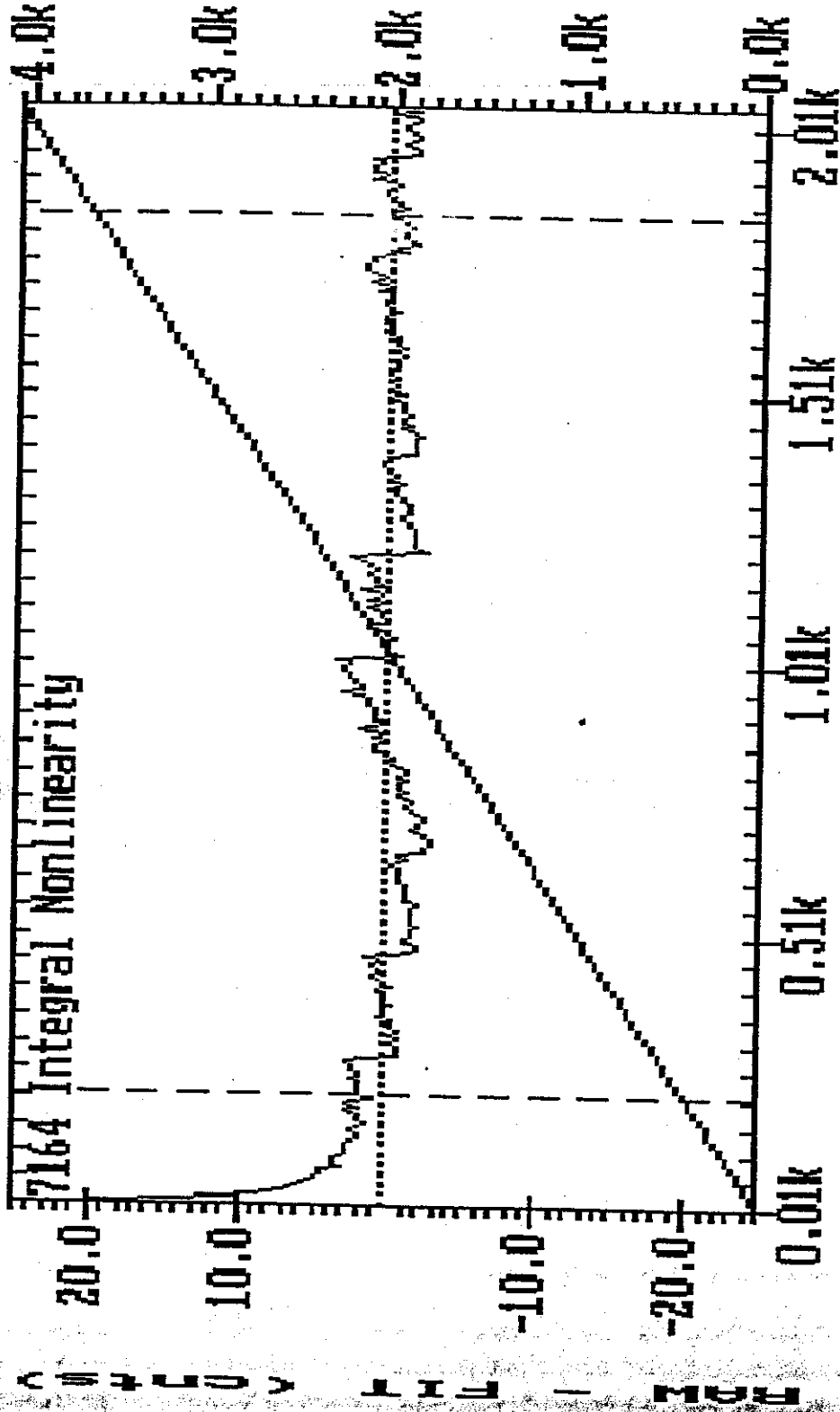
7164 Integral Nonlinearity

RAW DATA (cnts)

RAW - FIT (cnts)

Channel #

Ofst(cnts)=2.6   Mxcnts=4095   Pnts=256 Cyc/pnt= 3   Ped=0 cnts
Gain(xcnt/ycnt)=498.09 Mncnts= 44

PHILLIPS SCIENTIFIC Test Program 5/16/1996 13:18:43

7164 Differential Nonlinearity
7-bit dithering

NUMBER OF HITS

20.0k

18.0k

1,300k 1,320k 1,340k 1,360k 1,380k 1,400k
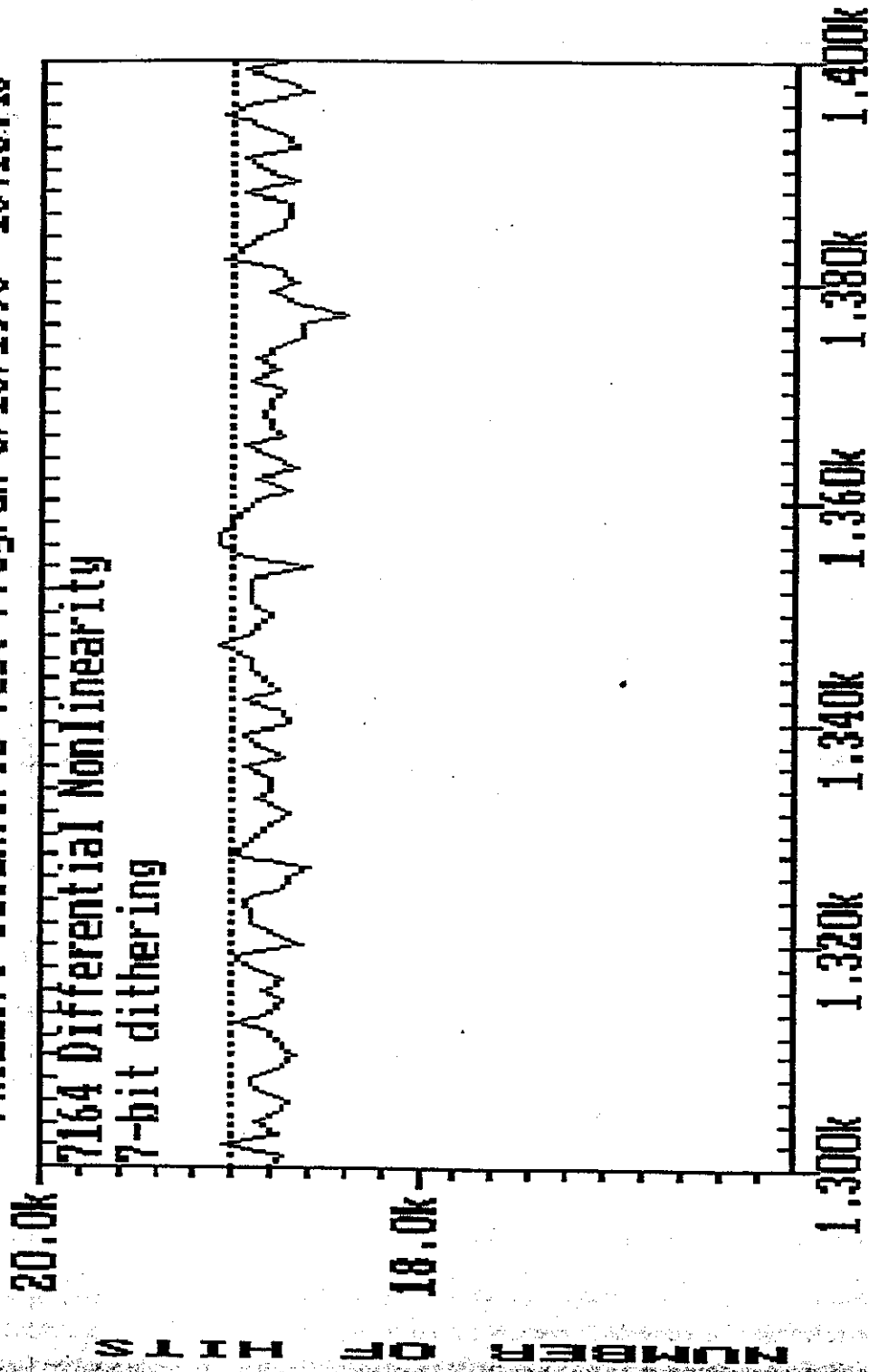
Histogram N=1896692   Average=18996.9   mxcnts=19067   Events=0
DNMissing Codes=0   DNL=+0.00/-0.03   mincnts=18397   Baseline=0

PHILLIPS SCIENTIFIC Test Program 5/16/1996 17:25:14

7164 Differential Nonlinearity
6-bit dithering

20.0k

18.0k

NUMBER OF HITS

1,300k   1,320k   1,340k   1,360k   1,380k   1,400k

HISTOGRAM BIN #

Channel 1
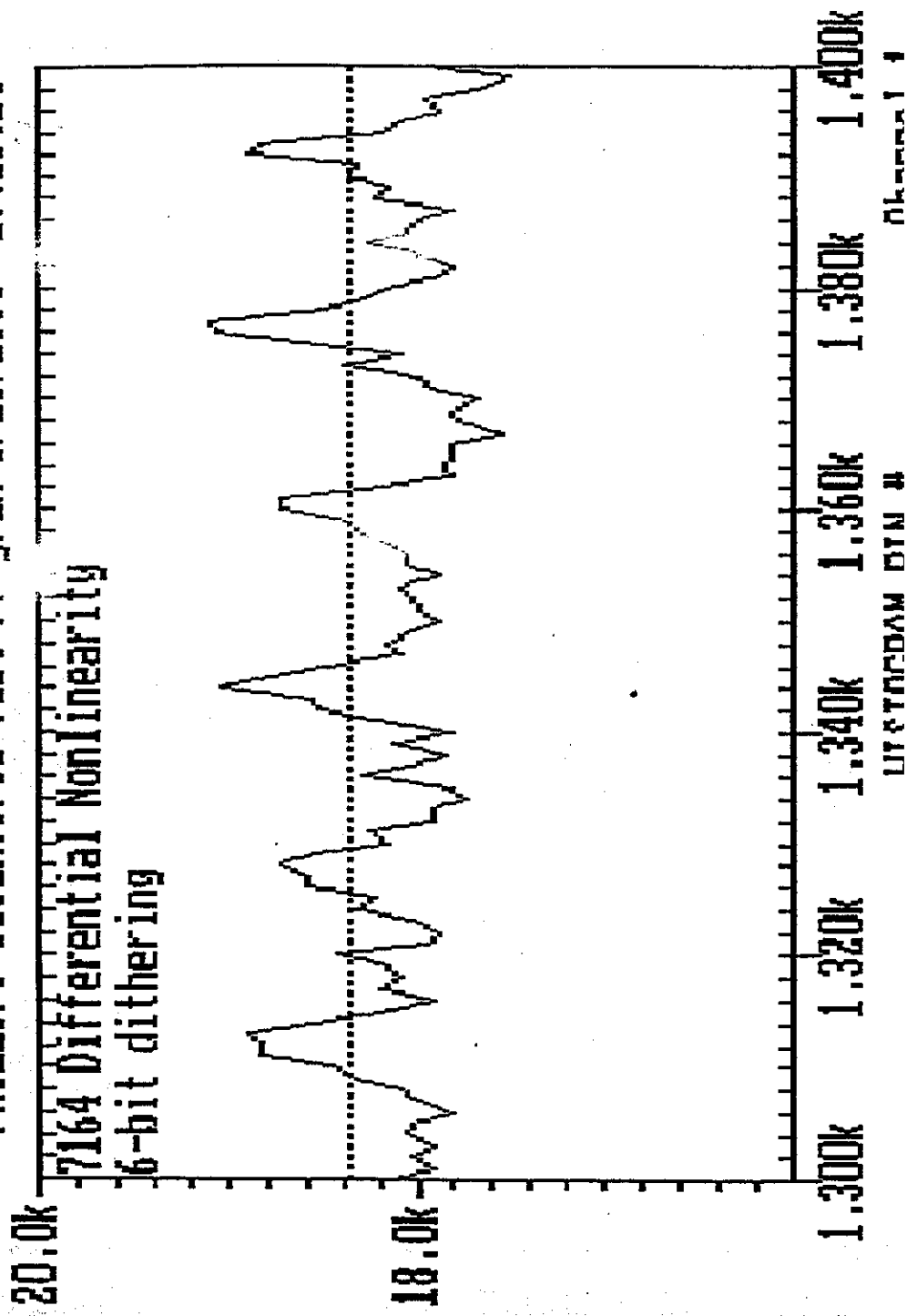
Histogram N=1835643   Average=18356.4   Mxcnts=19107   Events=0
0 Missing Codes   DNL=+0.04/-0.05 Mincnts=17502   Baseline=0

PHILLIPS SCIENTIFIC Test Program 5/19/1996 10:29:39

7164 Differential Nonlinearity
Dithering disabled

14.0k

12.0k

NUMBER OF HITS

1.300k   1.320k   1.340k   1.360k   1.380k   1.400k

Channel #

Channel #
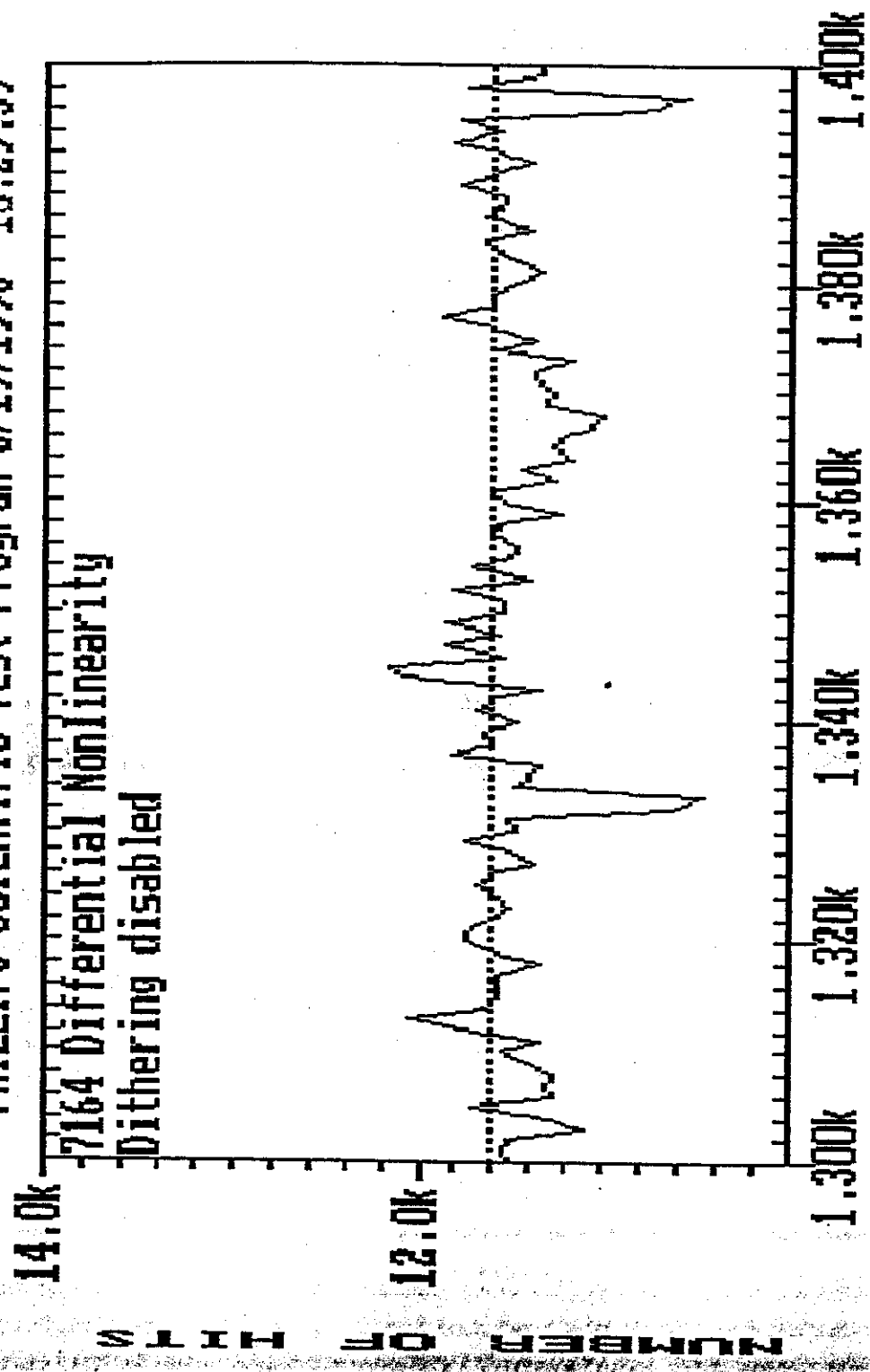
Average=1611.0 mxcnts=12140   Events=0
DNL=+0.05/-0.10 mincnts=10454 Baseline=0

Histogram N=1161100
0 Missing Codes