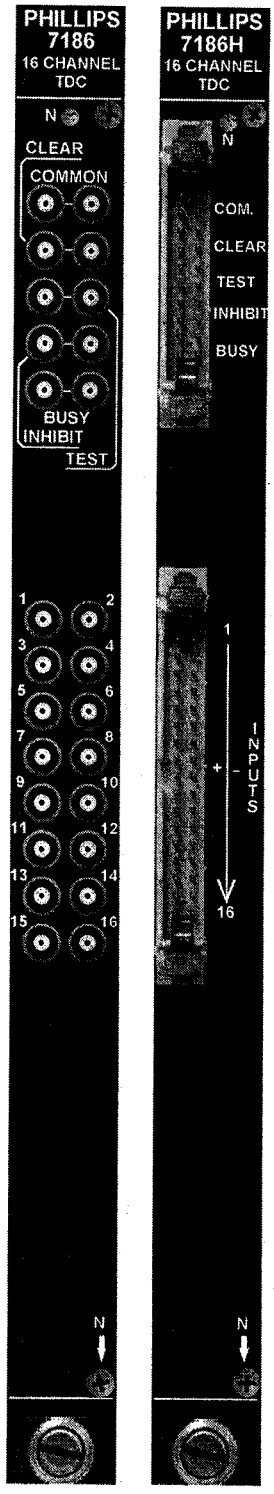
Phillips Scientific

16 Channel Time to Digital Converter

CAMAC MODEL 7186 7186H

FEATURES

* Model 7186 Features NIM Inputs with LEMO Connectors
* Model 7186H Features Differential ECL Header Connector Inputs
* Less Than 7.2 µSec Conversion and Processing Time
* 12-Bit Dynamic Range, Resolution down to 25pSec/Count
* Programmable Pedestal Correction
* Sparse Data Scan with Lower and Upper Time Cuts
* Fast CLEAR and INHIBIT
* COMMON START or COMMON STOP
* Built-in Test Features Check TAC and Digitization



DESCRIPTION

The Model 7186/H TDC implements 16 channels of Time to Amplitude Conversion (TAC) followed by a digital processing section and CAMAC interface in a single width CAMAC module. To minimize data readout time, the module performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following the COMMON input. It may be delayed by a user-programmable amount to allow time for derivation of fast CLEAR signals.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel fast CLEAR or CAMAC Clear commands.

Four user selectable time ranges are provided in a given configuration:

Standard Configuration	
Range	Resolution
100 nSec	25 pSec
200 nSec	50 pSec
400 nSec	100 pSec
800 nSec	200 pSec

Alternate Configuration	
Range	Resolution
1 µSec	.25 nSec
2 µSec	.50 nSec
4 µSec	1.0 nSec
8 µSec	2.0 nSec

Note: All channels need not have the same scale factors. Custom ranges are available when ordering.

INDIVIDUAL START or STOP INPUTS

7186 : Fast negative NIM, direct-coupled input, (50 ohm impedance); Minimum pulse width 10nSec.

7186H : 100 ohm, differential ECL, 100mV threshold. Minimum input pulse width 10nSec.

COMMON, CLEAR, INHIBIT and TEST INPUTS

7186 : Two bridged LEMO inputs to facilitate daisy chaining, (5.1K ohm impedance). Terminate at end of chain with 50 ohms.

7186H : Two pairs of differential ECL inputs to facilitate daisy chaining. Terminate at end of chain with 110 ohms.

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Conversion Time : *Less than 7.2µSec, includes 750nSec prior to digitization for settling and for accepting CLEAR signals. Conversion is triggered by the leading edge of COMMON. Digitization may be delayed by 0 to 16µSec in 62.5nSec increments with external jumpers. An increased delay is mandatory in the slower ranges of COMMON START mode and may be used in either mode to allow a greater acceptance window for CLEAR signals. For ranges above 800nSec full scale, increasing the delay by more than 4µSec after the first STOP may result in a degradation in module performance.*

CLEAR Input : *Resets the Hit Register and the front ends as follows:*

100, 200, 400, 800nSec ranges:

t < (Common - 850nSec): *Resets any channels that have received START signals; no effect on digitization.*

(COMMON - 700nSec) < t < Start of Digitization: *Resets front ends and aborts digitization cycle.*

t > Start of Digitization: *Resets front ends; no effect on digitization.*

1, 2, 4, 8µSec Ranges:

t < (COMMON - 2.2µSec): *Resets any channels that have received START signals; no effect on digitization.*

(COMMON - 1.9µSec) < t < Start of Digitization: *Resets front ends and aborts digitization cycle.*

t > Start of Digitization: *Resets front ends; no effect on digitization.*

BUSY is asserted following CLEAR to allow time for the front ends to fully reset.

INHIBIT : *Inhibits TAC and digitization. Must be removed at least 10nSec before START or COMMON signals for those signals to be recognized. To inhibit the front ends, INHIBIT must be applied no later than the START signal. To inhibit digitization, INHIBIT must be present 10nSec before COMMON.*

TEST Input : *Applies STOP/START signal to all channels. Used in conjunction with the COMMON START/STOP input to test operation of the TDC anywhere within the selected range.*

BUSY Output

7186 : *LEMO output connector. Double amplitude NIM current switching bridged output (32mA).*

7186H : *Differential ECL output. Two double row connector pins.*
Active as follows:

- *From receipt of COMMON until the event has been aborted by CLEAR or has been fully digitized and read out through the sparse data port. BUSY follows the Hit Register and thus may also be released by clearing the Hit Register.*
- *For 800nSec following fast CLEAR (2.4µSec for ranges greater than or equal 1µSec)*
- *During any CAMAC addressing of the module.*

FRONT END PERFORMANCE

A dithered mode may be selected by the user for improved performance for spectroscopy analysis. It should be disabled when working within the bottom or top 1.5% of the module's range or for those measurements not creating histograms of data.

Linearity : *Integral : Less than 4 counts over 10% to 90% of range.*
Differential : Less than 0.025% of full scale maximum.
Non-Dithered: ± 0.5 bins typical DNL.
Dithered: ± 0.1 bins typical DNL.

FRONT END PERFORMANCE (continued)

Noise, Jitter : Typically less than 20 pSec RMS.

Crosstalk : Less than 3 LSB between adjacent channels.

START/STOP Pedestal : 20nSec internal offset; Front ends are offset by this amount for improved linearity and to allow use of full dynamic range.

Stability : Gain : 100 ppm/ °C typically. Offset : 0.15 counts/ °C typically.

Power Supply Requirements :
+ 6V @ 2.7 Amp typically
- 6V @ 2.2 Amp typically
+24V @ 180 mA typically
Forced air cooling is recommended.

ADDITIONAL TEST FEATURES

Calibration Check : Simulates a START/STOP sequence under CAMAC control to verify operation of the module. CAMAC selectable nominal 1/3 or 2/3 full scale calibration for each full scale range. Not intended for use in calibrating the module.

CAMAC Check : Loads a predetermined pattern to simulate the outputs of the A/D converters. Useful for verifying the operation of the digital processing sections of the module.

SPARSIFICATION and LAM OPERATION

Separate pedestals and upper and lower thresholds may be set for each channel. They are enabled using bits in the Control Register. Pedestals in signed 2's complement format are added to the data before threshold comparison. Bits in the Hit Register are set during digitization for those channels whose pedestal corrected data falls within their upper and lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data reads present only those channels with bits set in the Hit Register, starting with the highest numbered channel. As channels are read, their Hit Register bits are reset; when the final channel has been read LAM is reset. LAM is also reset when the Hit Register is reset.

DATA WORD FORMAT

16 13	12 1
Channel ID	Channel Data

CONTROL REGISTER FORMAT

16 9	8 4	3	2	1
Conversion Delay (Read Only)	0	UT Enable	LT Enable	PED Enable

CAMAC DATAWAY OPERATIONS

F(0)·A(X) : Read event data memory for Channel (X+1). Data word as described above.

F(1)·A(X) : Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).

F(4)·A(0) : Read Sparse Data. Only those channels with data that falls between their upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.

F(6)·A(0) : Read the Control Register. Format described above.

CAMAC DATAWAY OPERATIONS (continued)

F(6)·A(1) : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.

F(8) : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(9) : Clears the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(10) : Clears LAM. Occurs on S2 strobe. The address lines have no effect on this command.

F(11)·A(0) : Reset the Control Register. Occurs on S2 strobe.

F(11)·A(1) : Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11)·A(2) : Reset the Test Register. Occurs on S2 strobe.

F(11)·A(3) : Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.

F(16)·A(X) : Write to data memory for channel (X+1).

F(17)·A(0) : Select the Pedestal Memory for the next F1 or F20 operation.

F(17)·A(1) : Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)·A(2) : Select the Upper Threshold Memory for the next F1 or F20 operation.

F(17)·A(4) : Select the Test Register for the next F20 operation.

F(19)·A(0) : Set the Control Register bits. Format described above.

F(20)·A(X) : Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is ±4095; threshold ranges are 0 to 4095.

Program the test register if it was selected by the most recent F17 operation.

A0 : Test pattern = 001001001001
A1 : Test pattern = 010010010010
A2 : Test pattern = 100100100100
A3 : Test pattern = 111111111111

F(23)·A(0) : Reset the Control Register bits. Format described above.

F(24) : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(25)·A(0) : Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.

F(25)·A(1) : Test. Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)·A(2) : Test. Runs a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

F(26) : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

C, Z : Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I : Inhibits TDC Front End.

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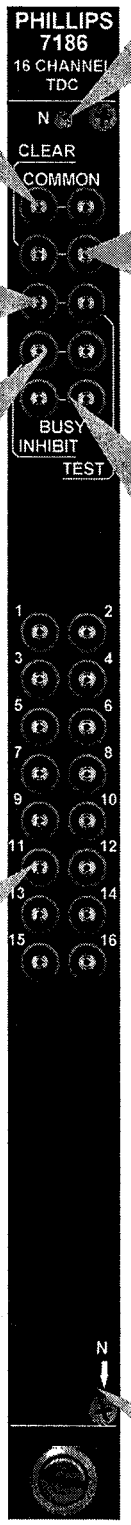
MODEL 7186 SIXTEEN CHANNEL 12-BIT TIME TO DIGITAL CONVERTER

(Front Panel Description)



Common Input: NIM Logic (-500mV); Bridged Inputs Allow Easy Daisy Chaining; Configured for Either Common Start or Stop.

An LED Indicates the Module is Being Addressed via CAMAC.

Clear Input: NIM Logic (-500mV); Bridged Inputs Allow Easy Daisy Chaining; Clears All TDC Front Ends.

Test Input: NIM Logic (-500mV); Bridged Input Allow Easy Daisy Chaining; Generates a Start and StopTest Event to All Channels.

Inhibit Input: NIM Logic (-500mV); Bridged Inputs Allow Easy Daisy Chaining; Must Precede Common or Start by 10nSec.

Busy Output Active From Common until Clear or Event Read; Bridged NIM Out; -32mA (-1.6V @ 50 ohm, -.8V @ 25 ohm Load).

Sixteen Individual Start/Stop Inputs; NIM Level (-500mV), 50 ohm Input; Times Digitized from Common Input.

Standard #1 CAMAC Packaging in accordance with EUR 4100.

Notes:

1) Setup Internal Jumpers for Common START or Common STOP Operation.
2) Internal Jumper Selects One of Four Full Scale Time Ranges.
3) Rear Panel Jumper Provides a Programmable Conversion Delay of 16μSec in 62.5nS Increments. The Delay allows an Unwanted Event to be Cleared Before it is Digitized and Stored.

PROGRAMMING MANUAL FOR

THE MODELS

7164 / 7164H

7166 / 7166H

7167 / 7167H

7186 / 7186H

7187 / 7187H

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PROGRAMMING MANUAL FOR MODELS

7164/7164H,

7166/7166H, 7167/7167H,

7186/7186H, AND 7187/7187H

1. CAMAC DATAWAY OPERATIONS

1.1 Writing Data

F(16)•A(X): Write to data memory for channel (X+1).

1.2 Reading Data

F(0)•A(X): Read event data memory for Channel (X+1). Data word contains pedestal corrected data and the channel number. Data is present regardless of sparsification and is read non-destructively.

F(4)•A(0): Read Sparse Data. Only those channels with data that falls between the Upper and Lower Thresholds are read, starting with the highest numbered channel. Each read presents the next channel on the hit list. As each channel is read, its bit in the Hit Register is reset. Reading an empty buffer returns Q false, X true.

16 13	12 1
Channel #	Channel Data

Channel Data Format

1.3 Set the Control Register

F(19)•A(0)•D(X): Selectively enable the Pedestal, Upper and Lower Thresholds for all channels.

D1=1 Enable the Pedestals
D2=1 Enable the Lower Thresholds
D3=1 Enable the Upper Thresholds
D4 to D15 = 1 No Action

1.4 Reset the Control Register

F(23)•A(0)•D(X): Selectively disable the Pedestal, Upper and Lower Thresholds for all channels.

D1=1 Disable the Pedestals
D2=1 Disable the Lower Thresholds
D3=1 Disable the Upper Thresholds
D4 to D15 = 1 No Action

1.5 Read the Control Register

F(6)•A(0): Read the control register. This tells which of the Pedestal, Upper Threshold or Lower Threshold are enabled, as well as the programming of the Conversion Delay.

16 9	8 4	3	2	1
MSB Delay Time LSB	0	UT Enabled	LT Enabled	PED Enabled

Control Register Data Format

1.6 Read the Hit Register

F(6)-A(1): Read the Hit Register. Shows which channels' pedestal corrected data fall within their Upper and Lower Thresholds. A 1 in any position indicates the channel has passed sparsification. For example, 0100 0010 0000 1001 shows that data on channels 1, 4, 10, and 15 have passed sparsification. These are the channels which will be read using the sparse data read function (F4).

16	1
Channel 16	Channel 1

Hit Register Data Format

1.7 Read and Write the Parameter Memory

Signed two's complement arithmetic is used. Pedestals occupy 13 bits giving a range of -4096 ($1000) to +4095 ($0FFF). Thresholds are 12 bits, ranging from 0 to 4095.

1.7.1 Select the Parameter

F(17)-A(0): Select the Pedestal Memory for the next F1 or F20 operation.

F(17)-A(1): Select the Lower Threshold Memory for the next F1 or F20 operation.

F(17)-A(2): Select the Upper Threshold Memory for the next F1 or F20 operation.

1.7.2 Write the Data

F(20)-A(X): Write the Pedestal, Upper or Lower Threshold for Channel (X+1) as selected by the most recent F17 operation.

1.7.3 Read the Data

F(1)-A(X): Read the Parameter Memory pointed to by the most recent F17 operation for channel (X+1).

1.8 Test Functions

1.8.1 Run a Test from fhe Test Registers

1.8.1.1 Select a Pattern

1.8.1.1.1 Select the Test Registers

F(17)-A(4): Select the Test Register for the next F20 operation.

1.8.1.1.2 Select a Pattern

F(20)-A(X): Program the Test Register if it was selected by the most recent F17 operation.

X	Pattern
0	001001001001
1	010010010010
2	100100100100
3	111111111111

1.8.1.2 Run A Test

F(25)-A0: Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.

1.8.2 Run A Front End Full Scale Test

Models 7166/7166H, 7167/7167H, 7186/7186H and 7187/7187H

F(25)•A1: Initiates a data acquisition cycle using a simulated event of approximately 1/3 full scale applied to the front end.

F(25)•A2: Initiates a data acquisition cycle using a simulated event of approximately 2/3 full scale applied to the front end.

Model 7164/7164H

F(25)•A1: Initiates a data acquisition cycle using a simulated event of approximately 1/20 full scale applied to the front end.

F(25)•A2: Initiates a data acquisition cycle using a simulated event of approximately 1/4 full scale applied to the front end.

1.9 LAM

LAM is set during digitization when pedestal corrected data for at least one channel falls between that channel's Upper and Lower Thresholds.

F(24): Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(26): Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

F(8): Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(10): Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.

1.10 Resets

F(9): Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.

F(11)•A(0): Reset the Control Register. Occurs on S2 strobe.

F(11)•A(1): Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

F(11)•A(2): Reset the Test Register. Occurs on S2 strobe.

F(11)•A(3): Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.

2. CAMAC NON-DATAWAY COMMANDS

C, Z: Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.

I: Inhibits front end functions.

INDEX

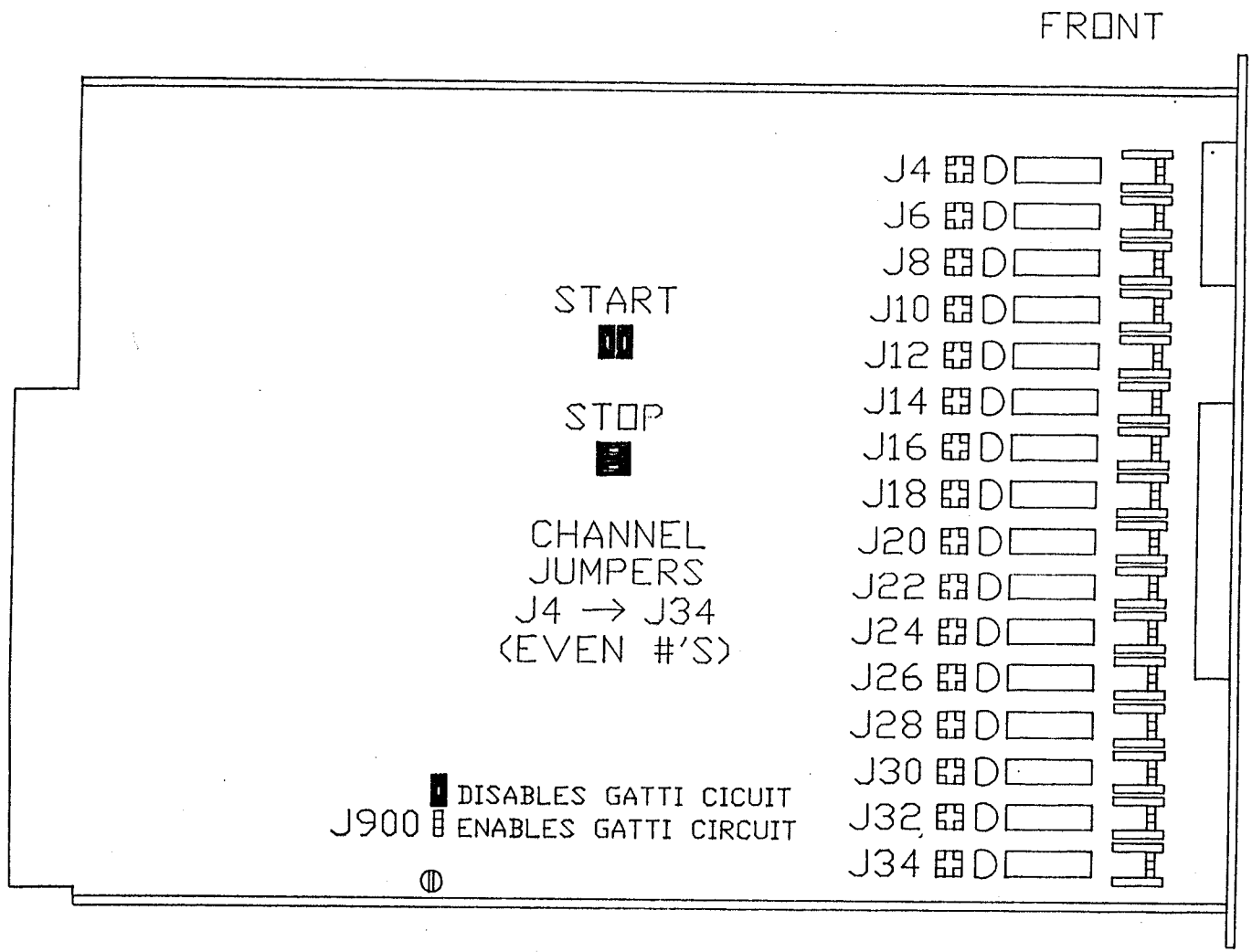
APPENDIX A

7186 / 7186H

PROGRAMMING

JUMPERS

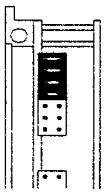
7186 JUMPER LOCATIONS

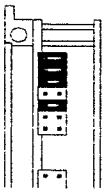


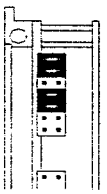
7186 JUMPER PROGRAMMING

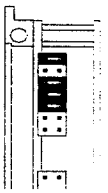
ALL VIEWS ARE FROM TOP REAR OF MODULE

RANGE

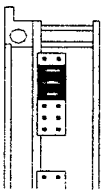

100 nsec

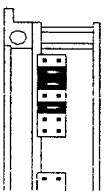

200 nsec

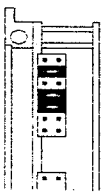

400 nsec

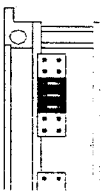

800 nsec

EXTENDED RANGE OPTION *


1 µsec

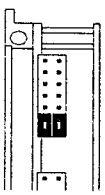

2 µsec

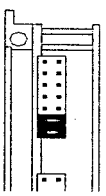

4 µsec


8 µsec

* THIS OPTION REQUIRES AN INTERNAL CAPACITOR VALUE CHANGE. CONSULT FACTORY FOR DETAILS.

COMMON START/STOP


COMMON START

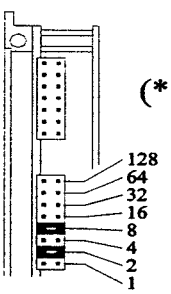

COMMON STOP

START

STOP

CHANNEL JUMPERS J4 - J34 (EVEN #'S)

CONVERSION DELAY

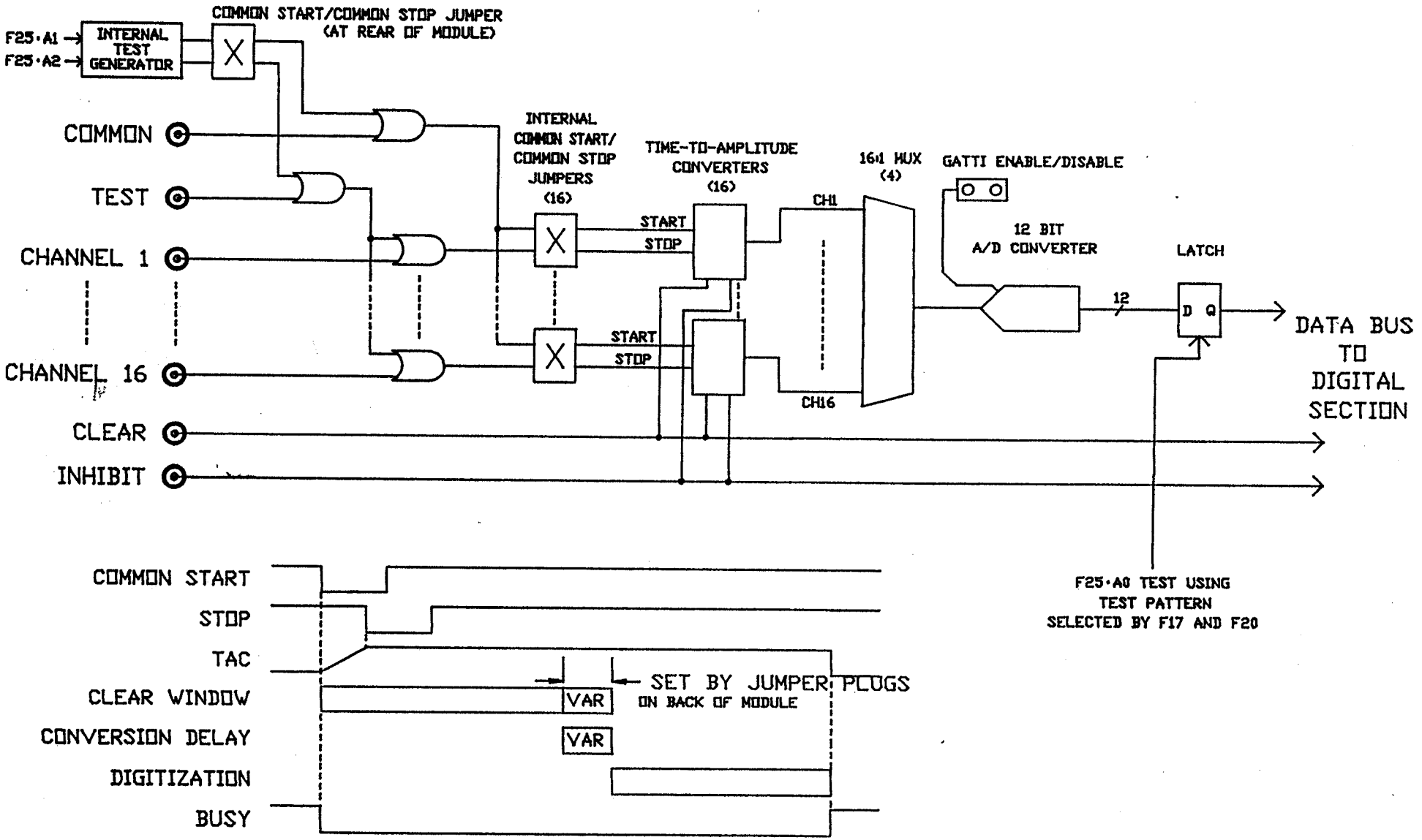


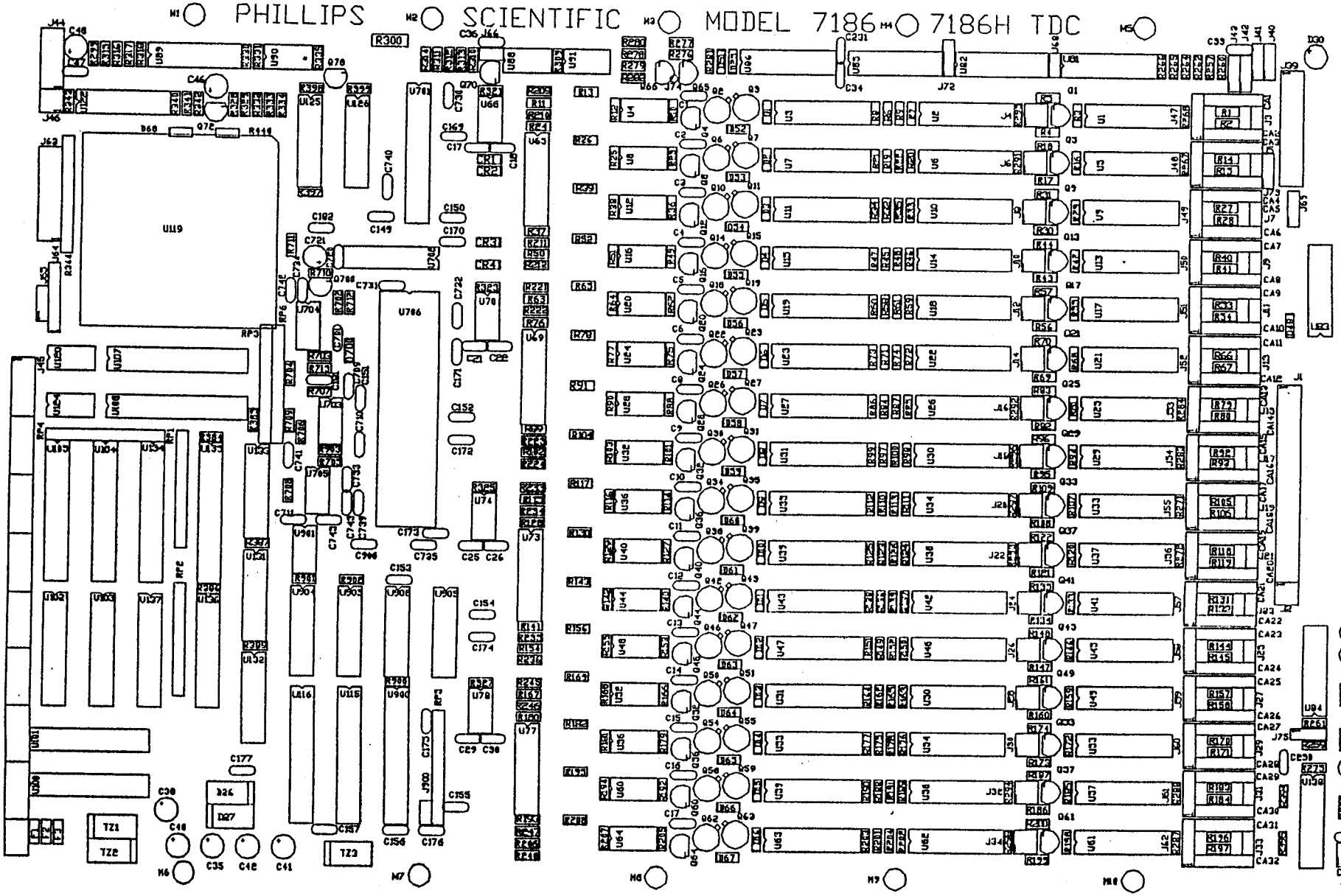
(*62.5 nsec)

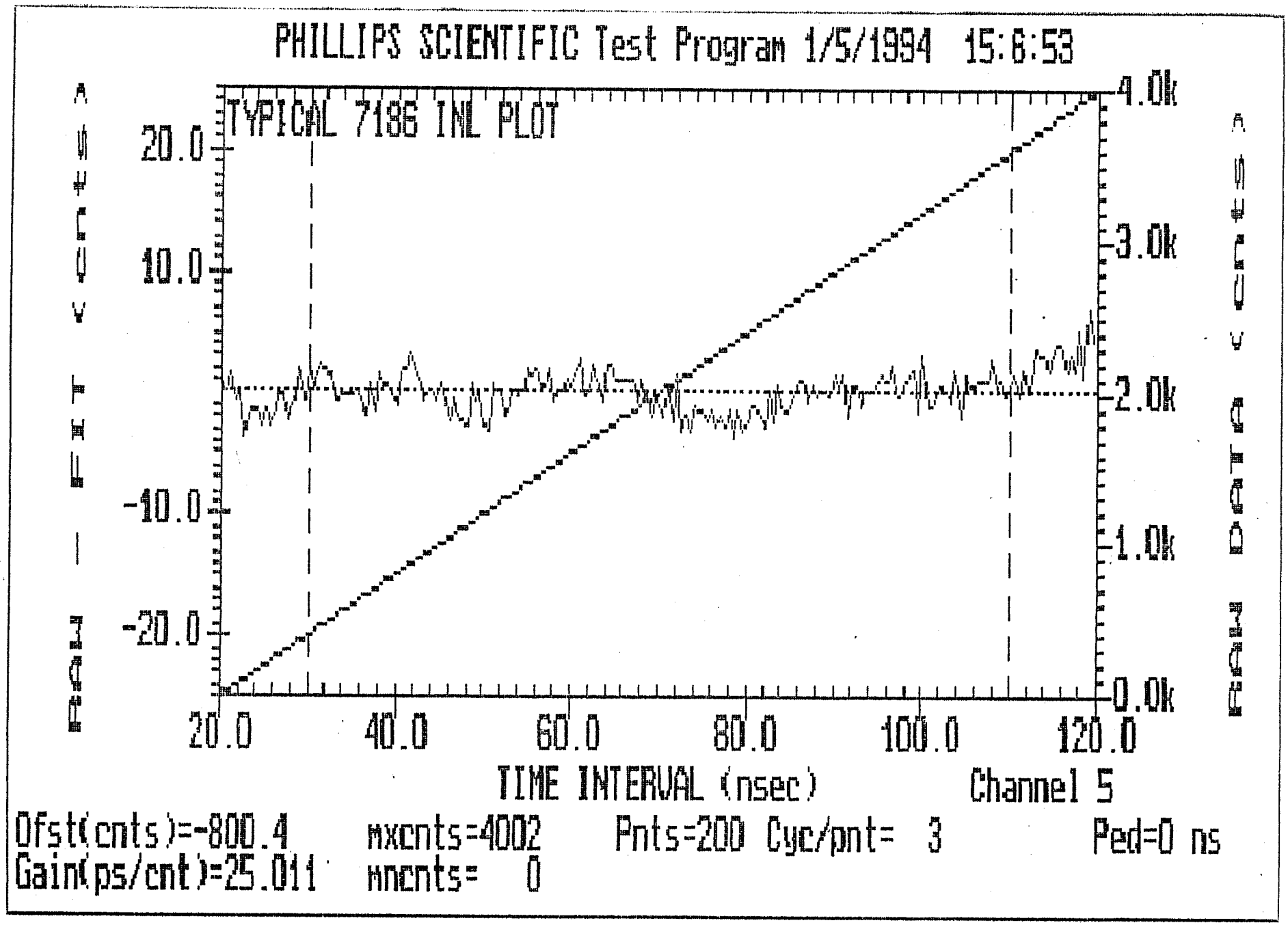
625 nsec SHOWN

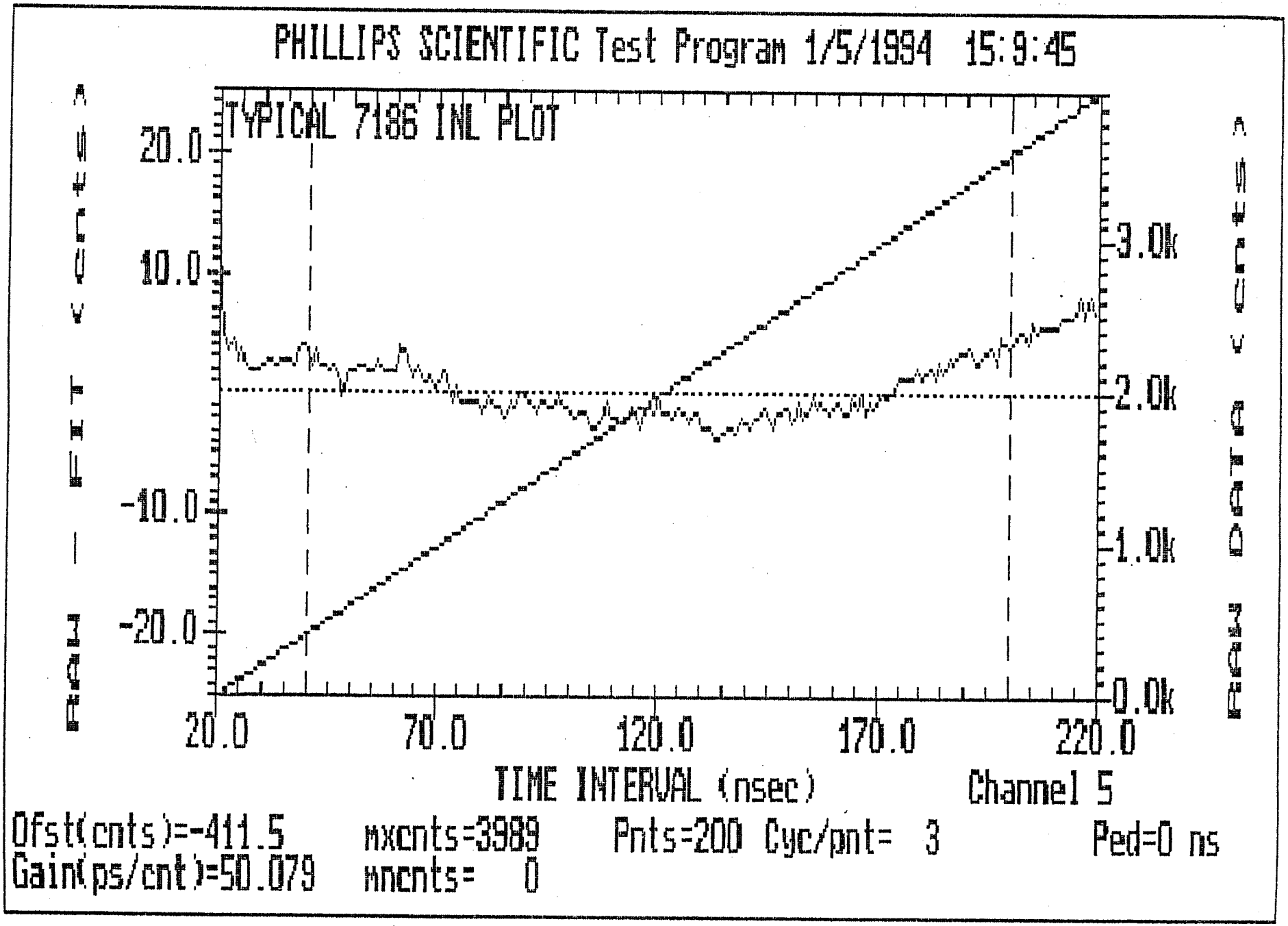
Minimum Conversion Delay required for 7186 COMMON START Mode as follows:

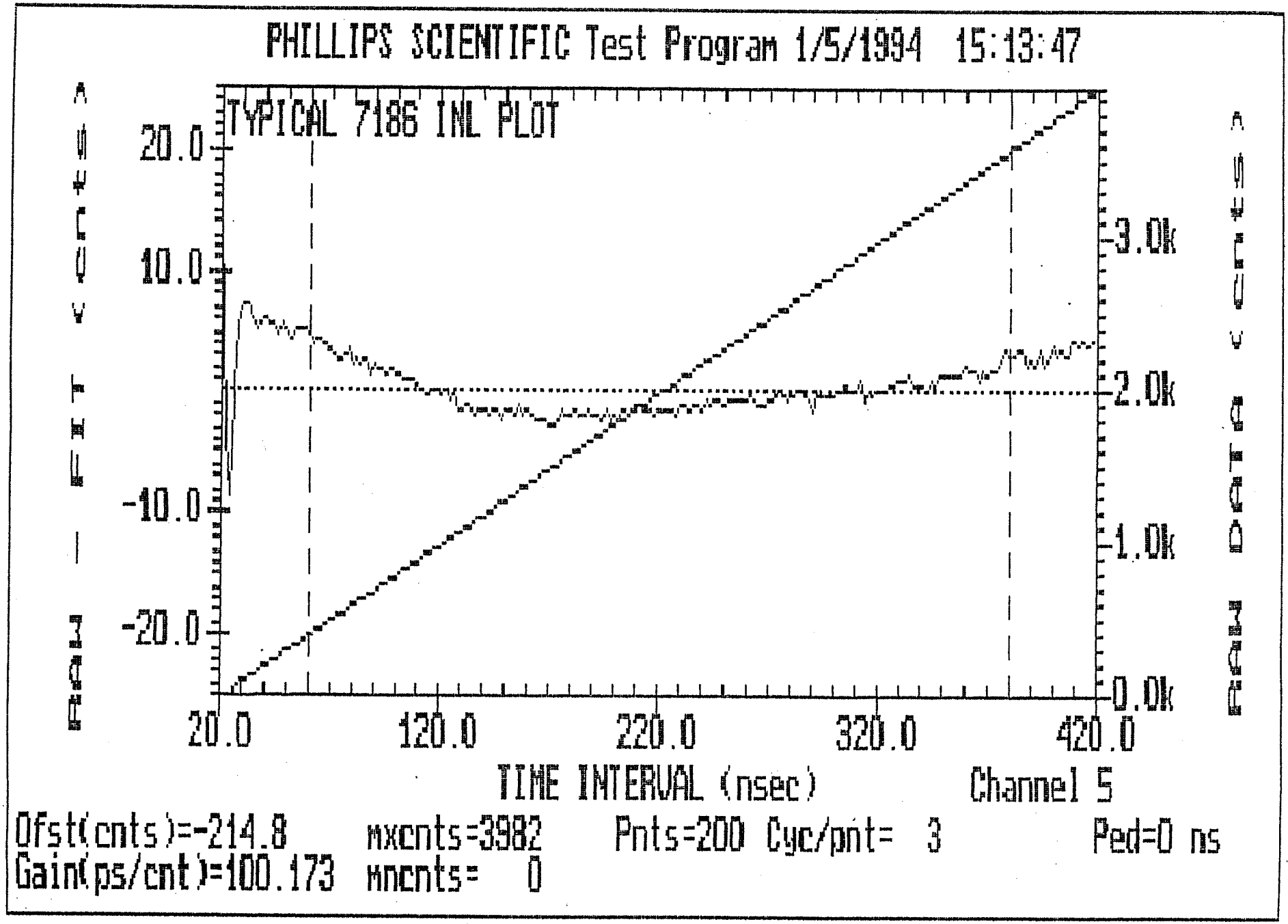
RANGE	DELAY	JUMPER POSITION
100 Nsec	0	-
200 Nsec	125 Nsec	2
400 Nsec	312.5 Nsec	4, 1
800 Nsec	750 Nsec	8, 4
1 µsec	937.5 Nsec	8, 4, 2, 1
2 µsec	1937.5 Nsec	16, 8, 4, 2, 1
4 µsec	3937.5 Nsec	32, 16, 8, 4, 2, 1
8 µsec	7937.5 Nsec	64, 32, 16, 8, 4, 2, 1
Other Ranges	≥ (Range - 100 Nsec)	

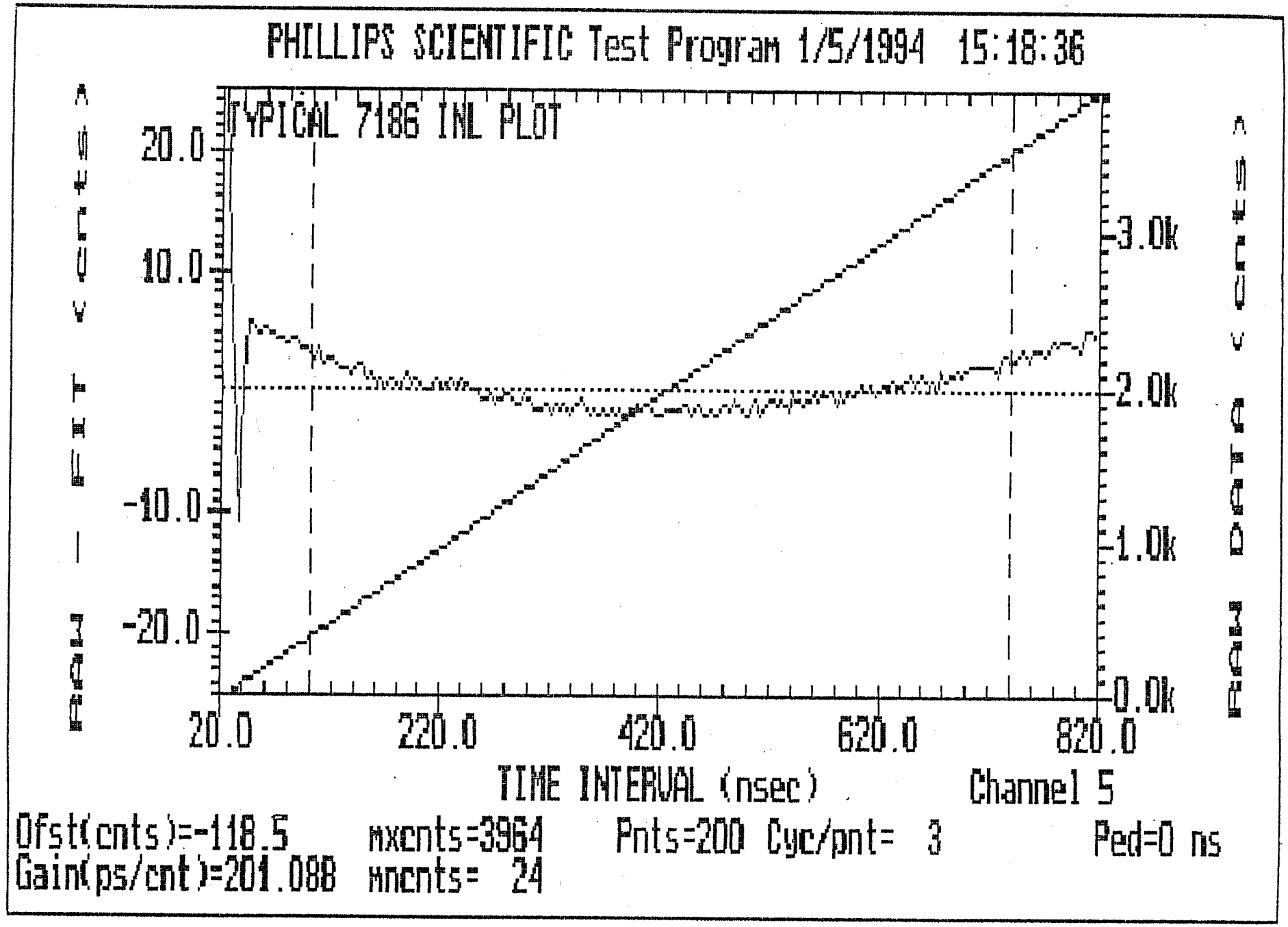

F25·A1
F25·A2
INTERNAL TEST GENERATOR
COMMON START/COMMON STOP JUMPER (AT REAR OF MODULE)
COMMON
TEST
CHANNEL 1
CHANNEL 16
CLEAR
INHIBIT
INTERNAL COMMON START/ COMMON STOP JUMPERS (16)
START
STOP
TIME-TO-AMPLITUDE CONVERTERS (16)
CH1
CH16
16:1 MUX (4)
GATTI ENABLE/DISABLE
12 BIT A/D CONVERTER
12
LATCH
D Q
DATA BUS TO DIGITAL SECTION
F25·A0 TEST USING TEST PATTERN SELECTED BY F17 AND F20
COMMON START
STOP
TAC
CLEAR WINDOW
CONVERSION DELAY
DIGITIZATION
BUSY
VAR
VAR
SET BY JUMPER PLUGS ON BACK OF MODULE

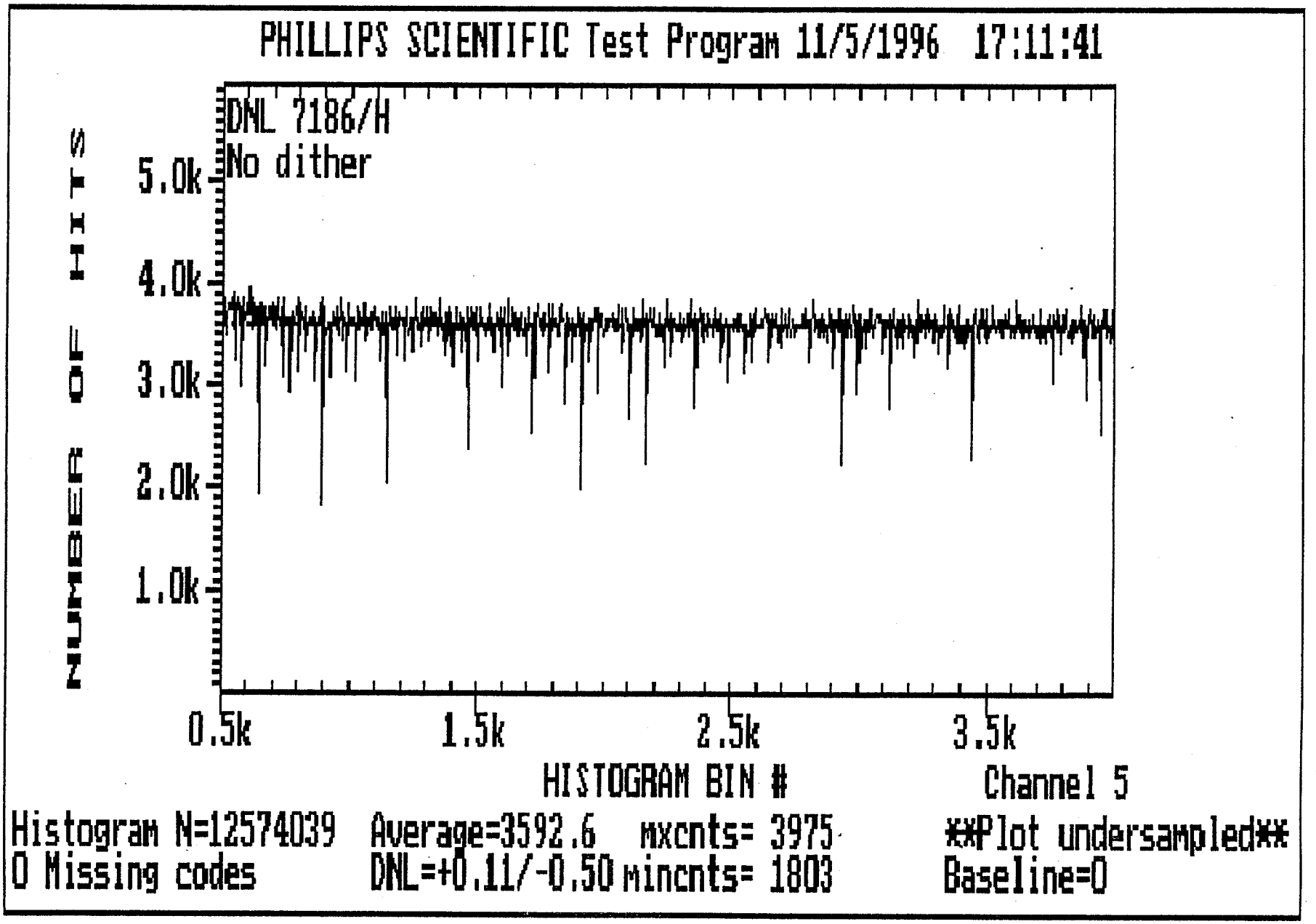

PHILLIPS SCIENTIFIC MODEL 7186 7186H TDC

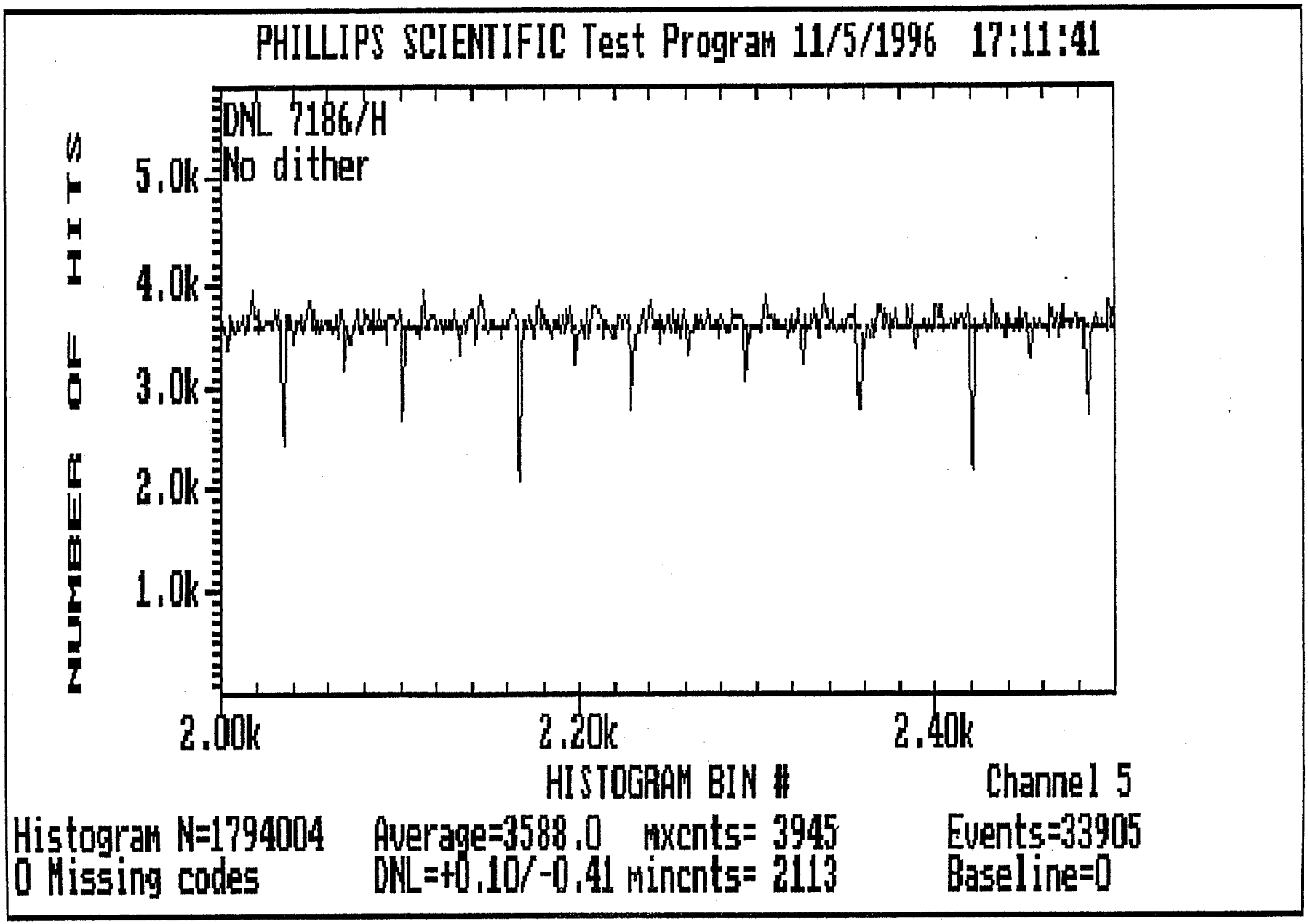

PHILLIPS SCIENTIFIC Test Program 1/5/1994 15:6:53
TYPICAL 7186 INL PLOT
Data - INL cnts
20.0
10.0
-10.0
-20.0
4.0k
3.0k
2.0k
1.0k
0.0k
Data peak cnts
20.0
40.0
60.0
80.0
100.0
120.0
TIME INTERVAL (nsec)
Channel 5
Ofst(cnts)=-800.4
Gain(ps/cnt)=25.011
mxcnts=4002
mncnts= 0
Pnts=200 Cyc/pnt= 3
Ped=0 ns

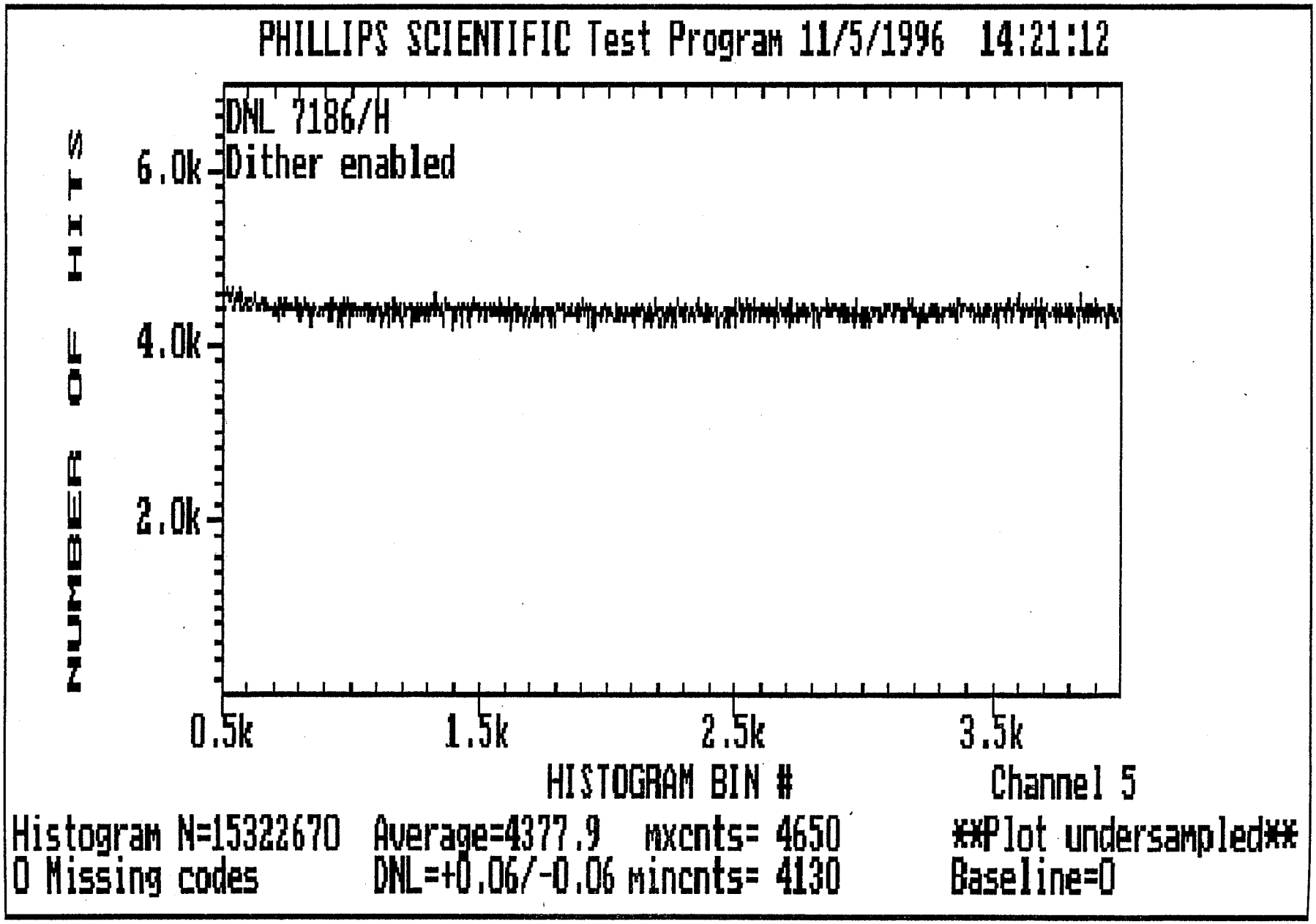

PHILLIPS SCIENTIFIC Test Program 1/5/1994 15:9:45
TYPICAL 7186 INL PLOT
Raw - Fit values
20.0
10.0
-10.0
-20.0
3.0k
2.0k
1.0k
0.0k
20.0
70.0
120.0
170.0
220.0
TIME INTERVAL (nsec)
Channel 5
Ofst(cnts)=-411.5
Gain(ps/cnt)=50.079
mxcnts=3989
mncnts= 0
Pnts=200 Cyc/pnt= 3
Ped=0 ns

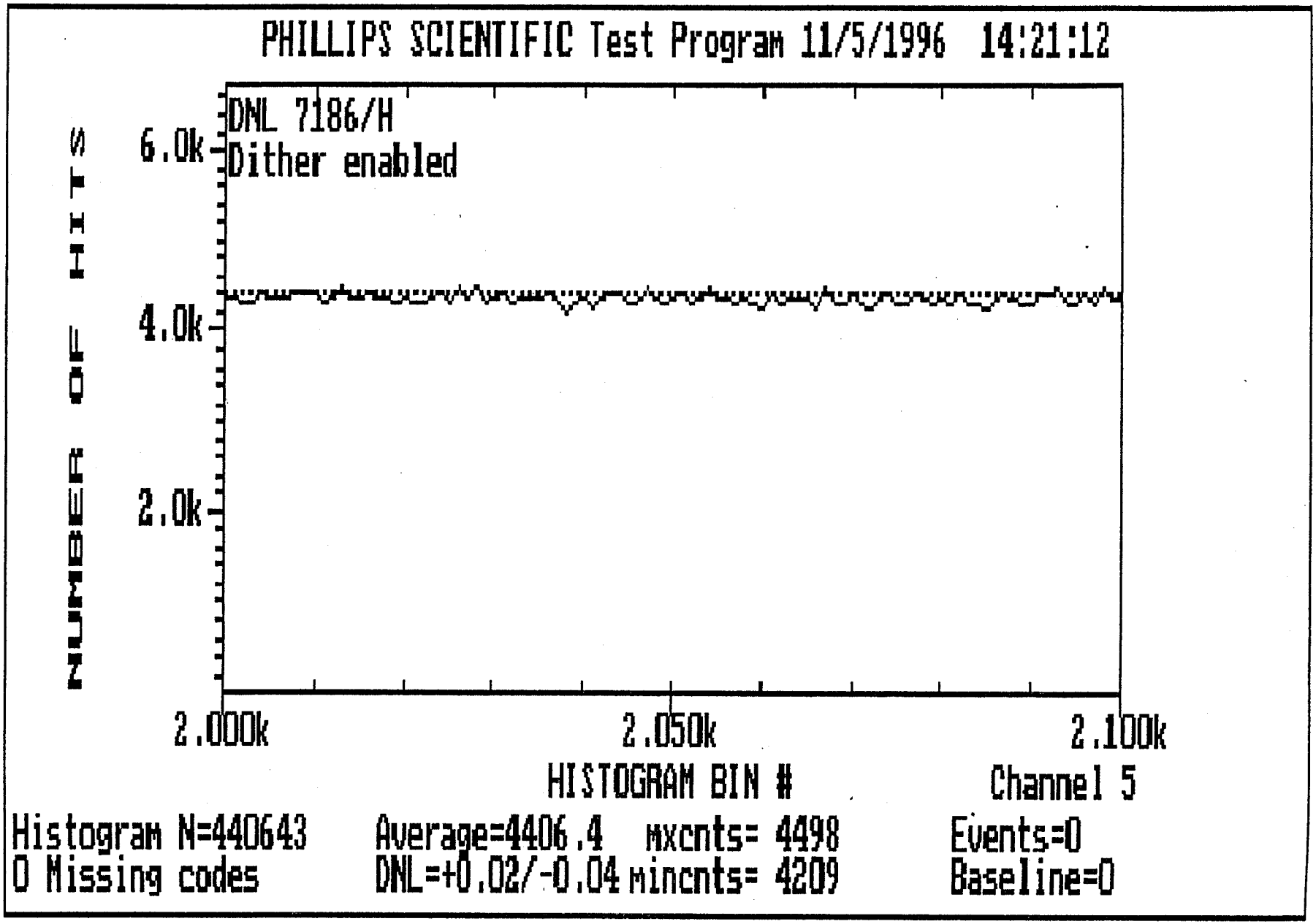

PHILLIPS SCIENTIFIC Test Program 1/5/1994 15:13:47
TYPICAL 7186 INL PLOT
20.0
10.0
-10.0
-20.0
3.0k
2.0k
1.0k
0.0k
20.0
120.0
220.0
320.0
420.0
TIME INTERVAL (nsec)
Channel 5
Ofst(cnts)=-214.8
Gain(ps/cnt)=100.173
mxcnts=3982
mncnts= 0
Pnts=200 Cyc/pnt= 3
Ped=0 ns

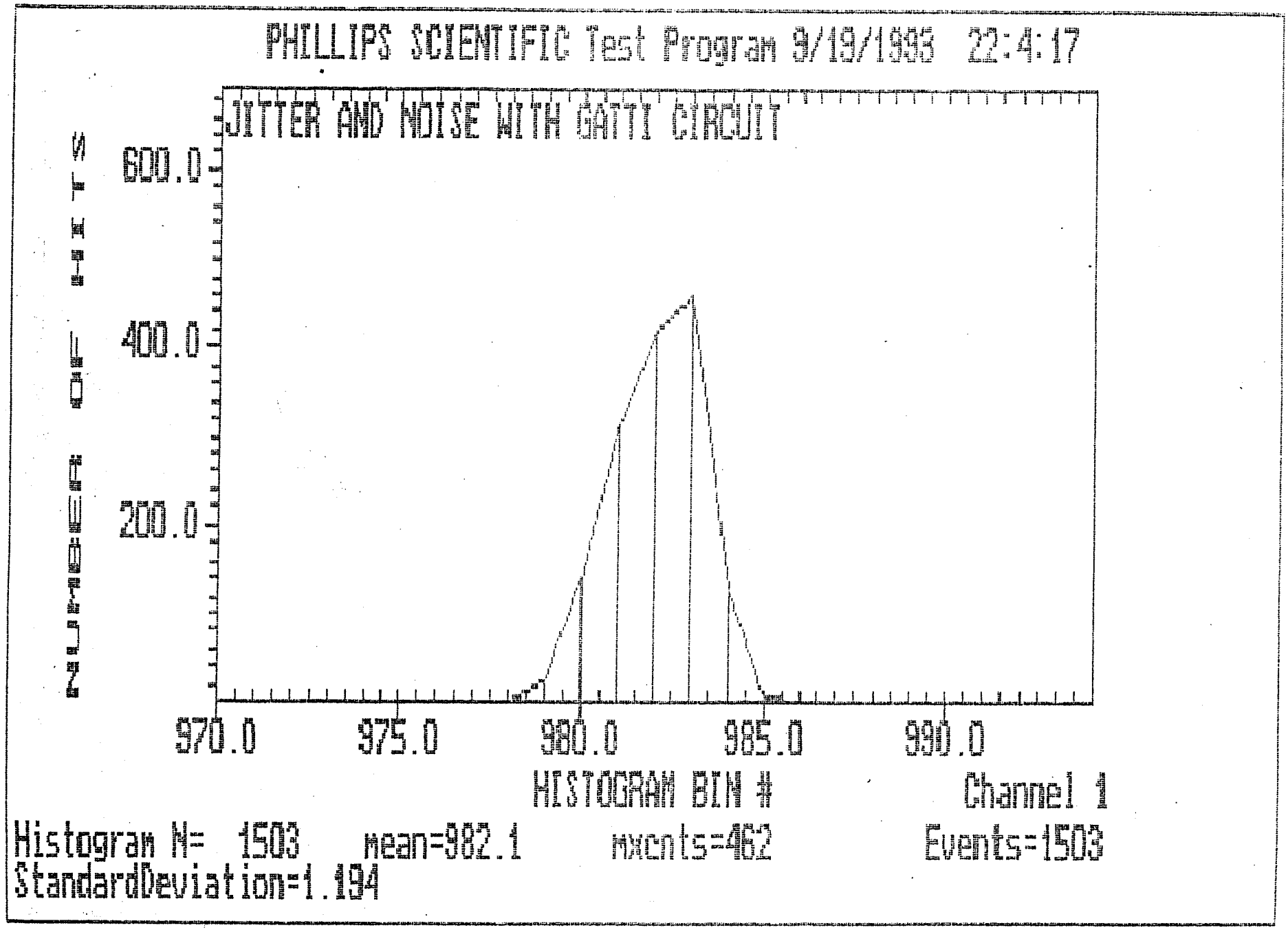

PHILLIPS SCIENTIFIC Test Program 1/5/1994 15:18:36
TYPICAL 7186 INL PLOT
Real - Fit vcnts
20.0
10.0
-10.0
-20.0
3.0k
2.0k
1.0k
0.0k
Real Data vcnts
20.0
220.0
420.0
620.0
820.0
TIME INTERVAL (nsec)
Channel 5
Ofst(cnts)=-118.5
mxcnts=3964
Pnts=200 Cyc/pnt= 3
Ped=0 ns
Gain(ps/cnt)=201.088
mncnts= 24

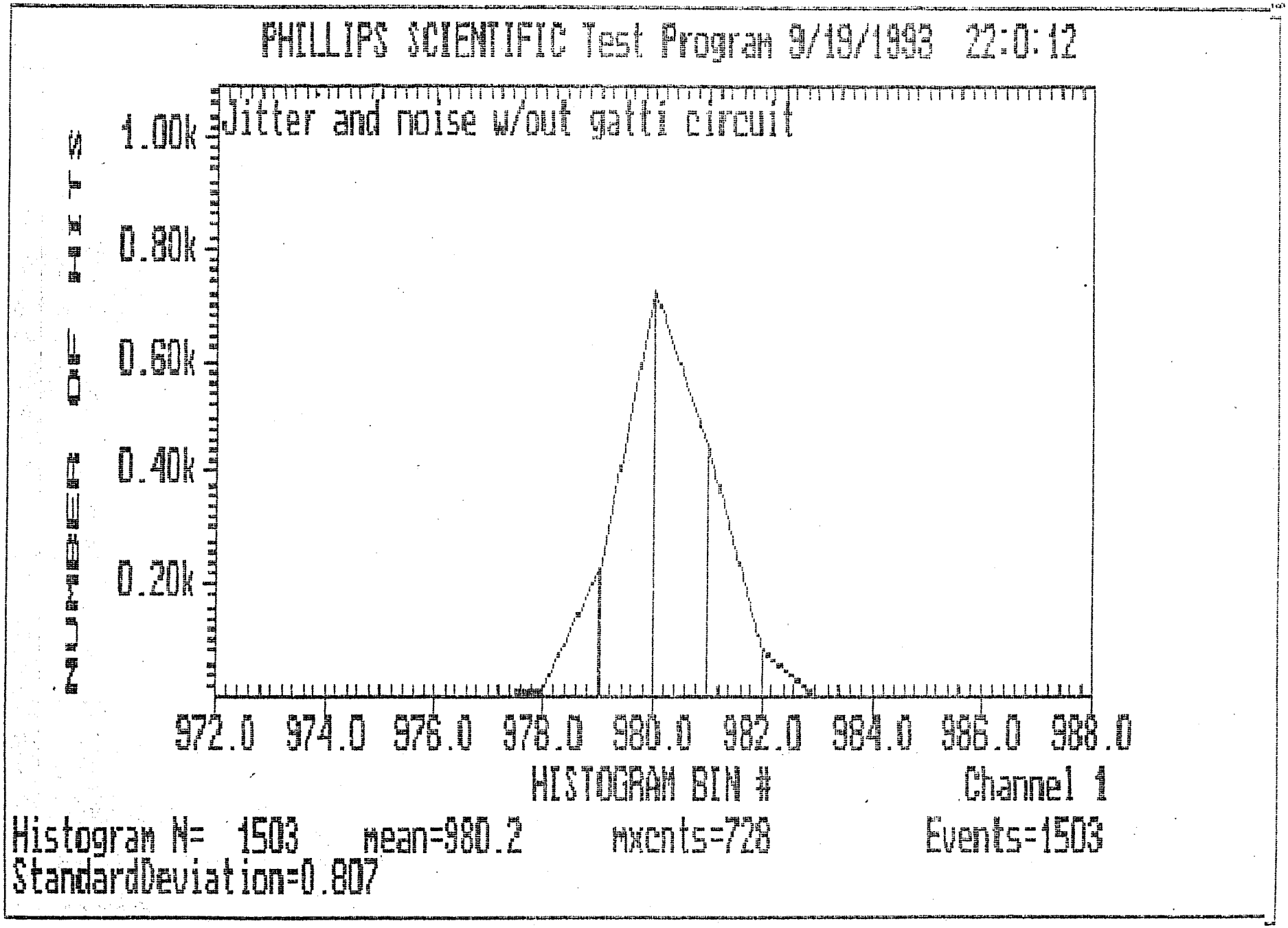

PHILLIPS SCIENTIFIC Test Program 11/5/1996 17:11:41
DNL 7186/H
No dither
NUMBER OF HITS
5.0k
4.0k
3.0k
2.0k
1.0k
0.5k
1.5k
2.5k
3.5k
HISTOGRAM BIN #
Channel 5
Histogram N=12574039 Average=3592.6 mxcnts= 3975 **Plot undersampled**
0 Missing codes DNL=+0.11/-0.50 mincnts= 1803 Baseline=0


PHILLIPS SCIENTIFIC Test Program 11/5/1996 17:11:41
DNL 7186/H
No dither
NUMBER OF HITS
5.0k
4.0k
3.0k
2.0k
1.0k
2.00k
2.20k
2.40k
HISTOGRAM BIN #
Channel 5
Histogram N=1794004
0 Missing codes
Average=3588.0
DNL=+0.10/-0.41
mxcnts= 3945
mincnts= 2113
Events=33905
Baseline=0


PHILLIPS SCIENTIFIC Test Program 11/5/1996 14:21:12
DNL 7186/H
Dither enabled
NUMBER OF HITS
6.0k
4.0k
2.0k
0.5k
1.5k
2.5k
3.5k
HISTOGRAM BIN #
Channel 5
Histogram N=15322670 Average=4377.9 mxcnts= 4650
0 Missing codes DNL=+0.06/-0.06 mincnts= 4130
Plot undersampled
Baseline=0


PHILLIPS SCIENTIFIC Test Program 11/5/1996 14:21:12
DNL 7186/H
Dither enabled
NUMBER OF HITS
6.0k
4.0k
2.0k
2.000k
2.050k
2.100k
HISTOGRAM BIN #
Channel 5
Histogram N=440643
0 Missing codes
Average=4406.4
DNL=+0.02/-0.04
mxcnts= 4498
mincnts= 4209
Events=0
Baseline=0


PHILLIPS SCIENTIFIC Test Program 9/19/1995 22:4:17
JITTER AND NOISE WITH GATTI CIRCUIT
NUMBER OF EVENTS
600.0
400.0
200.0
970.0
975.0
980.0
985.0
990.0
HISTOGRAM BIN #
Channel 1
Histogram N= 1503 mean=982.1 mxcnts=462 Events=1503
StandardDeviation=1.194


PHILLIPS SCIENTIFIC Test Program 9/19/1993 22:0:12
Jitter and noise w/out gatti circuit
NUMBER OF EVENTS
1.00k
0.80k
0.60k
0.40k
0.20k
972.0
974.0
976.0
978.0
980.0
982.0
984.0
986.0
988.0
HISTOGRAM BIN #
Channel 1
Histogram N= 1503 mean=980.2 mxcnts=728 Events=1503
StandardDeviation=0.807

PRODUCT WARRANTY

PHILLIPS SCIENTIFIC warrants its products to be free from defects in materials and workmanship and to meet performance specifications under normal use and operating conditions for a period of one year from the date of product shipment. The provisions of this warranty shall not apply to any product that has been subjected to misuse or which has been repaired or altered in any way by the purchaser.

Obligations under this warranty is hereby limited to the repair or replacement of the product, or part thereof, which is returned to Phillips Scientific within the warranty period. The foregoing constitutes the entire warranty in lieu of other warranties, expressed or implied, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose with respect to a product and the accompanying written materials. In no event will Phillips Scientific be liable for damages, including any loss of profits, or other direct, incidental or consequential damages arising out of use of or inability to use the product, even if Phillips Scientific or an authorized representative, agent or employee has been advised of the possibility of such damages. Phillips Scientific will not be liable for any such claim by any other party.

To obtain service under this warranty, the purchaser must in advance be issued a returned material authorization (RMA), and ship products prepaid to Phillips Scientific with documentation explaining the malfunction noted. The items will be evaluated, repaired or replaced and promptly returned prepaid if warranty claims are substantiated.