Amplifier (Tennelec TC241S)
CRDC 1 Anode
Uni. OUT
C. Gain 10
F. Gain 5.1
T. Gain 5
Fast OUT
R2C2S11
Amplifier (Tennelec TC241S)
CRDC 2 Anode
IN
Uni. OUT
C. Gain 10
F. Gain 6.5
T. Gain 5
Fast OUT
R2C2S12
Quad Fast Amplifier (NSCL)
S1: CRDC 1 Anode
S2: CRDC 2 Anode
R2C2S9
CFD (Canberra 454)
(22 ns)
CRDC 1
CRDC 2
R1C4S6
Variable Amplifier (LeCroy 612EM)
E1 up
E1 down
97: ???
91: From OBJ SCI
1 Right
1 Left
2 Right
2 Left
5 Left
6 Right
6 Left
R2C2S8
200
Splitter Att. (NSCL)
E1 u
E1 d
to FERA
1-11
R1C3S12
Fan In / Out (ESN LF 4000)
CRDC1
CRDC2
to stop TAC CRDC1
to XLM CRDC1
to Scaler and MTDC
to stop TAC CRDC2
to XLM CRDC2
R1C4S11
MCFD-16 (Mesytec)
E1 u
E1 d
A1900
OBJ SCI
R1C2S1
Fan In / Out (ESN LF 4000)
E1 u
E1 d
A1900
OBJ SCI
R1C2S3
to target area
ECL-NIM-ECL (NSCL)
RF
Hodosc 0-31
to Scaler and MTDC
R1C2S2
1: E1 up
2: E1 down
3: A1900
4: OBJ SCI
5: ???
6: RF
7: CRDC 1 an.
8: CRDC 2 an.
13: Hodosc.
16: S800 trigg
CC-USB (Wiener)
B2: Live Trigger
to ULM (C)
R1C1S24
MTDC-32 (Mesytec)
0: E1 up
1: E1 down
2: A1900
3: OBJ SCI
4: ???
5: RF
6: CRDC 1 anode
7: CRDC 2 anode
12: Hodosc.
15: S800 trigg
Trig 0
B3: ADC gate
R2C1S2
ULM (LeCroy 2367)
A1: S800 trigger source (E1 up)
A2: Secondary trigger source
A3: External source (Trig Insp 4)
A7: Gretina synch (Fast Patch 3)
A8: Gretina clock (Fast Patch 1)
C1: VM-USB: 01 (Busy 1)
C2: CC-USB: O1,O2 (Busy 2)
C8: CC-USB: O1,O2 (Time stamp latch)
B2: Live Trigger
B3: ADC Gate
B4: QDC Gate
B5: TDC Start
B6: Trigger Register Gate
B8: Live Trigger
B9: Insp. 1
B10: Insp 2
B11: Insp 3
B12 Insp 4
B13: Fast Clear
B16: Time stamp clock
D1: S800 source
D2: Seconday source
D5: S800 trigger
D6: Coinc. Trigger
D7: Ext. trigg. 1
D8: Ext. trigg. 2
D9: Second trigg.
D10: Raw trigg.
D11: Live trigg.
D12: Raw pulser
D13: Live pulser
D14: Fast clear
D15: 10 Hz
D16: 1 Hz
C9: Time stamp clock
C10: Time stamp latch
R1C1S17
16-ch CFD (LeCroy 4413)
B5: TDC Start
B13: Fast Clear
B4: QDC gate
veto
sync
to Phillips ITDC
Clear and Gate to FERA
R1C1S20
CFD (CAEN C671)
Hodoscope 16-23
Hodoscope 24-31
R1C1S14
Hodoscope 0-7
Hodoscope 8-15
R1C1S12
Coinc. Register (LeCroy 4448)
B8: Live Trigger
Gate
R1C1S13
Net Controler (CAEN V288)
Serial line to CAEN shapers hodoscope + ion chamber
R2C1S21
XLM (JTEG)
R2C1S4
TAC (ORTEC 566)
S800 Trigger (200 ns)
300
62: From OBJ SCI CFD dU6
R2C2S1
60: From Galotte CFD dU6
R2C2S3
B5: TDC Start
CRDC 1 Anode
R2C2S2
Scaler (LeCroy 4434)
17: E1 up
18: E1 down
19: A1900
20: OBJ SCI
22: RF
23: CRDC 1 anode
24: CRDC 2 anode
29: Hodosc.
32: S800 trigg
R1C1S16
XLM72 V
PPACs
R2C1S116
ADC (Phillips 7164)
B3: ADC gate
94/04: Target
CRDC1 anode
CRDC2 anode
TAC (E1,CRDC1)
TAC (E1,CRDC2)
TAC (XF SCI,E1)
TAC (OBJ SCI,E1)
TAC (Gallote,E1)
TAC(E1,Hodoscope)
R1C1S23
XLM (JTEG)
1: E1 up del.
3: E1 down del.
9: E1 up del.
10: EXT 1
12: Gretina gamma OR (Fast P 2)
13: Cyclotron RF
14: OBJ SCI del.
15: XF SCI del.
Del
R2C1S7
ECL-NIM-ECL (NSCL)
Hodoscope 0-15
Hodoscope 16-31
E1 up
E1 down
to XLM Del. (Phillips TDC)
S800 Trigger E1 up
EXT 1
Gretina gam OR (Fast P 2)
67/37: OBJ SCI del. (data-U6)
XF_SCI del.
R1C3S7
Gate Generator (NSCL)
CC-USB: 02
to OR with O1
R1C2S4
Random Pulse Gen. (NSCL)
Scale Down (NSCL)
Fan In / Out (ESN LF 4000)
E1 up
Pulser
Gretina gamma OR (Fast Patch 2)
EXT 1
EXT 2
to XLM Del. (Phillips TDC)
61/31: to S800 FPD Rate Meter
to start TACs
to ULM (A)
R1C3S9
Fan In / Out (NSCL)
UNPLUGGED
1000
66/36: XF SCI del. (data-U6)
Hodosc 0-16
Hodosc 17-31
to #107 patch. target area
to TAC
R1C2S6
ECL-NIM-ECL (NSCL)
1-4: from XLM Delay
to ULM (A)
64/34: Delay Inspect 1
65/35: Delay Inspect 2
R1C2S7
VM-USB (Wiener)
B2: Live Trigger
R2C1S1
TAC (ORTEC 566)
S800 Trigger
A1900
R1C2S4
FERA (LeCroy 4300B)
B13:Fast Clear
B4: QDC gate
1: E1_u (200 ns)
2: E1_d (200 ns)
R1C1S18
XLM72
1: Live Trigger
2: CRDC 1 Anode
R2C1S10
ECL-NIM-ECL (EG&G-ESN EC1600)
to XLM PPACs
ULM I/O (B)
B2: Live Trigger
B3: ADC Gate
B4: QDC Gate
B5: TDC Start
B6: Coinc. Reg. Gate
B8: Live Trigger
B9: Insp. 1
B10: Insp 2
B11: Insp 3
B12 Insp 4
B13: Fast Clear
B15: Go
gate to FERA
55/25: Trigg. Insp. 1
56/26: Trigg. Insp. 2
57/27: Trigg. Insp. 3
58/28: Trigg. Insp. 4
to clear FERA
to #106 (target patch.)
R1C3S11
Fan In / Out (NSCL)
70/40: A1900
XF SCI
MCFD
Stop TAC
CC-USB: O1
CC-USB: O2
to ULM (C)
S800 Trigger
Start TAC (E1,Galott.)
109/19: S800 source to Target area
69/39: Cyclotron RF
R1C2S5
Gate Generator (NSCL)
Gretina clock (Fast patch 1)
Hodosc 0-31
to Scaler and MTDC
to Anticoinc. Hodos.
to Start TAC Hodos.
R1C3S5
Logic Unit (Phillips 755)
NOT(B6: Coinc. Reg. gate)
S800 Trigger (100 ns)
S800 Trigger
Hodoscope 0-31
AND(Hodoscope 0-31, NOT(S800 Trigger))
NOT(S800 Trigger
R1C3S6
100
TAC (ORTEC 566)
B5: TDC Start
CRDC 2 Anode
R2C2S5
TDC (Phillips 7186H)
B5: TDC Start
Common
R1C1S23
XLM72V
1: Live Trigger
2: CRDC 2 Anode
R2C1S13
Fan In / Out (ESN LF 4000)
to start TAC CRDC1
to start TAC CRDC2
to Phillips TDC
B5: TDC Start
B6: Coinc. Reg. Gate
B8: Live Trigger
B3: ADC Gate
to veto RF
to XLM CRDC1
to XLM CRDC2
to veto TAC start (S800 trigg - OBJ)
to Fast patch 4: MasterLive (data-U6)
to MTDC trig0
to ADC Gate
R1C2S10
Fan In / Out (LeCroy 429A)
B3: ADC Gate
B2: Live Trigger
Gates to ADCs Hodos.
to I1 CC-USB
to I1 VM-USB
UNPLUGGED (PULSER)
R1C2S11
ECL-NIM-ECL (NSCL)
B8: Gen. more trigg. live signals
B8: Live Trigger
CRDC 1 Anode
CRDC 2 Anode
B3: ADC Gate
VM-USB: O1
CC-USB: O1,O2
1,2 to XLM CRDC1
3,4 to XLM CRDC2
5,8 Gates to ADC Hodos.
9 to ULM C1: VM-USB: 01
10 to ULM C2: CC-USB: O1,O2
16 to ULMC8: CC-USB: O1,O2
R1C3S10
Logic Unit (Phillips 752)
Start TAC (E1,OBJ)
Start TAC (E1, XF)
R2C2S10
TAC (ORTEC 566)
S800 Trigger
R2C2S6
ADC (Phillips 7164H)
Live Trigger
Hodoscope 1-16
R1C1S8
Hodoscope 17-32
R1C1S7
Ion. Chamber (from Shaper Amplif.)
R1C1S6
CRDC
Gretina Time stamp Clock (Fast P 1)
Gretina Sync (Fast Patch 3)
Cyclotron RF
S800 Trigger
A1900
Pulser
OBJ SCI
Det # 1 target
Det # 3 target
Det # 4 target
Gretina gam OR (Fast Patch 2)
E1 up
E1 down
Galotte
Hodoscope
XF_SCI
ULM
ECL signals (Flat cable)