Centre d'Etudes Nucléaires de Bordeaux Gradignan Chemin du Solarium Le Haut Vigneau BP 120 F-33175 GRADIGNAN Cedex



J. Pibernat

Service Electronique & Acquisition mailto:pibernat@cenbg.in2p3.fr

## Minutes of the 11/25 2008 ASAD meeting at IRFU (Saclay)

## Meeting purpose:

- 1. Technical subjects
  - a) System definition
  - b) Subsystem definition
    - i. AGET settings and controls
    - ii. ASAD controls
    - iii. Data Management & Multiplicity
  - c) Detector interface
    - i. Detector/ASAD connection
    - ii. ZAP (input protections)
    - iii. Cooling
  - d) CoBo interface
- 2. Project management subjects
  - Planning
  - ASAD tests
  - Tasks to be done

## Meeting associates:

From CENBG: J.L. Pedroza, J. Pibernat From GANIL: G.Wittwer From IRFU: P. Baron, E. Delagnes, F Druillole, J. E. Ducret, E. Pollacco From MSU: A. Bickley, B. Lynch, N. Usher (joined by phone during part of the meeting)

# Meeting Summary:

## 1. Technical subjects

## a) System definition

ASAD (ASic-ADc) board is the part of GET situated between the detector (TPC) and the digital electronics which relates with data acquisition and control processes.

The main functionality of ASAD is to provide the ASIC AGET with all conditions required to make it operate properly.

Basically AGET samples the signals coming from the TPC, and records them in analogue memories which are readout when particular events occur.

These events are met when the triggers given by each channel of AGET correspond with a user defined logical pattern (multiplicity). The analogue data are then readout and converted in digital data by ASAD, before being transferred to CoBo (COncentration BOard).

To perform all its tasks (settings and tests of AGET, part of the multiplicity building, data conversion and transfer, etc.), ASAD is segmented in the following subsystems

## b) Subsystem definition

### • AGET settings and controls

ASAD will provide AGET with power supplies and all analogue current/voltage sources required to work properly.

AGET slow control (to set preamplifiers gain, shapers peaking time, threshold levels etc.) will be achieved via CoBo, by using a basic SPI protocol.

### ASAD own controls

ASAD should include the means to:

• Be identified in the whole GET system

This could be achieved according to a tagging format which specifies a board ID number, a serial number, a board release number, and the type of detector for which the board is set (proposed by G. Wittwer).

• Manage the power supplies

The aim of this functionality is to switch on or off, one particular ASAD board when required. As suggested by F. Druillole other functionalities could be added (current and/or voltage level check) if necessary, provided that the system is kept sufficiently "low power", sufficiently dense (room is a key feature in ASAD design), and sufficiently elementary to be tested easily

- Check the temperature at which ASAD is operated
- Test AGET or calibrate its channels

As presented by P. Baron AGET (AGET\_ASAD\_November08.ppt) can be operated according to 3 modes: Calibration, Test or Functional. In each mode, an external pulse generator based on a fast DAC can be used. This one should be included in ASAD. A dedicated input has to be assigned in ASAD to trigger at the same time all the pulsers embedded in each board. In this operating mode it will be useful to synchronize the AGET writing/reading clock and the pulsers trigger, that is a reason why the clock should be applied using a connector independent of the one that will be used to interface ASAD and CoBo. The protocol used to control the preceding parameters is not defined, but it could be useful to keep the same as the one planed for AGET slow control, i.e. a basic SPI protocol, by far simpler to implement than canbus for example.

#### • Data management

There are two types of data to handle: One that will be used to build the trigger multiplicity and one that will carry energy and 3<sup>rd</sup> dimensional position measurements.

#### Measurements

Before digitizing the data that relate to energy and position measurements, the ADC resolution has to be chosen. A 12 bits ADC should be convenient (despite E. Pollacco wishes!). The ADS6422 proposed by N. Usher which operates at 25MHz is an interesting choice as its power consumption is lower than the ADC used in the FEC boards and as it is able to carry out a better parallelization in the conversion process.

Its drawback is that its use implies to upgrade the firmware developed at IRFU for the T2K experiment. The conversion process has also to be checked. Is it a sample and hold based ADC or a track and hold based ADC? The answer to this question is very important as in one case the conversion process requires one clock period, and only a half of the clock period in the other case. The ADC data sheet does not give information on this subject, the ADC must be tested then.

#### • Multiplicity

To build the multiplicity a digital solution is chosen. E. Delagnes suggests to use the same ADC to convert during the memory writing process, the AGET outgoing signals present on the or-wired trigger line and to convert during the the memory reading process, the sampled analogue signals. This solution will enable to keep the same components and the same signals paths for both writing and reading processes, with the great benefits of lowering the power consumption, as well as preserving space, without reducing speed of operations.

To make this possible an analogue multiplexor has to be inserted in the AGET diagram which will switch the right signals to be converted depending on the actual process. P. Baron will implement this solution to check if the noise level is kept sufficiently low under these conditions. It is also noticed that the clock period to write and read the sampled data cannot be uncorrelated if this solution is approved.

#### c) Detector interface

#### Detector/ASAD connection

A solution based on the use of customized flex-circuits is proposed to connect ASAD boards to the TPC's (Bx\_TPC.ppt). This solution should enable to manufacture only one type of ASAD for all experiments and thus to lower the cost of manufacturing. Only the flex-circuits form-factor could be adapted according to the mechanical constraints in a particular experiment. The flex could host the ZAP circuitry studied at IRFU.

### ZAP (input protections)

About this study E. Delagnes reports that a problem occurred in the manufacturing of After and thus no tests on these ASIC hardness to sparks have been achieved (not enough spares). Another chip made of diodes and capacitors is developed at the moment at IRFU, the possibility to use it in GET will be considered.

#### Cooling

About the front-end cooling, some additional information are required before choosing a cooling system (volume in which ASAD boards will be mounted and pressure at which they will be operated). Detectors specifications have to be written.

#### d) CoBo interface

N. Usher presents a summary of the I/O that constitute the ASAD-CoBo interface. Everybody agrees the fact that these I/O have to be specified and approved as soon as possible in order to build the CoBo firmware. By writing ASAD specifications this interface will be more clearly defined.

#### 2. Project management subjects

#### Planning:

AGET submission to foundry should be reached at about June 2009.

ASAD prototype has then to be ready at September 2009, as well as the first release of the CoBo firmware in order to start the tests of AGET.

#### **ASAD Tests:**

F. Druillole suggests that the first release of ASAD be as similar as possible with the actual FEC, to implement part of the CoBo firmware into the actual FEM dedicated to test the FEC.

Generally, to save time in GET development it will be useful to reuse all existing hardware, so the FEC diagrams for example, will be transferred to CENBG in order to design ASAD.

#### Tasks to be done:

E. Pollacco will gather information about the mechanics in each experiment, to define the place where ASAD will be implemented

G. Wittver makes the link between ASAD workgroup and Multiplicity workgroup to give information about the multiplicity.

P. Baron will implement the analogue multiplexor in AGET and simulate the noise response.

J. Pibernat will discuss with manufacturers the feasibility of PCB based high density pad detectors. J.L. Pedroza and J. Pibernat will start to write the first release of ASAD specification.

Documents of the meeting will be uploaded at MSU wiki

Next ASAD meeting planed for January 2009 Next GET meeting planed for March 2009 (where?)