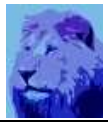
GET PROJECT

AsAd
(Asic-Adc)



SPECIFICATION

Version draft
2008, Dec

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CENBG

*At the ACTAR workshop held at Bordeaux in June 2008, it was decided to start a new multi-projects multi-laboratories collaboration to provide TPCs used in several laboratories (CENBG, GANIL,MSU,R3B, RIKAIN) with electronics for signals processing in the late 2012. This new system: **GET**, for **G**eneral **E**lectronics for **T**PCs is composed of several subsystems, as shown Figure 1 and covers signal processing from the detector to the data storage. The goal of this document is to specify the front end electronics AsAd (**As**ic-**Ad**c) which will be connected to the detectors and will send, after digitalisation, the data flow to the others subsystems.*
Any comment and suggestion can be sent at:

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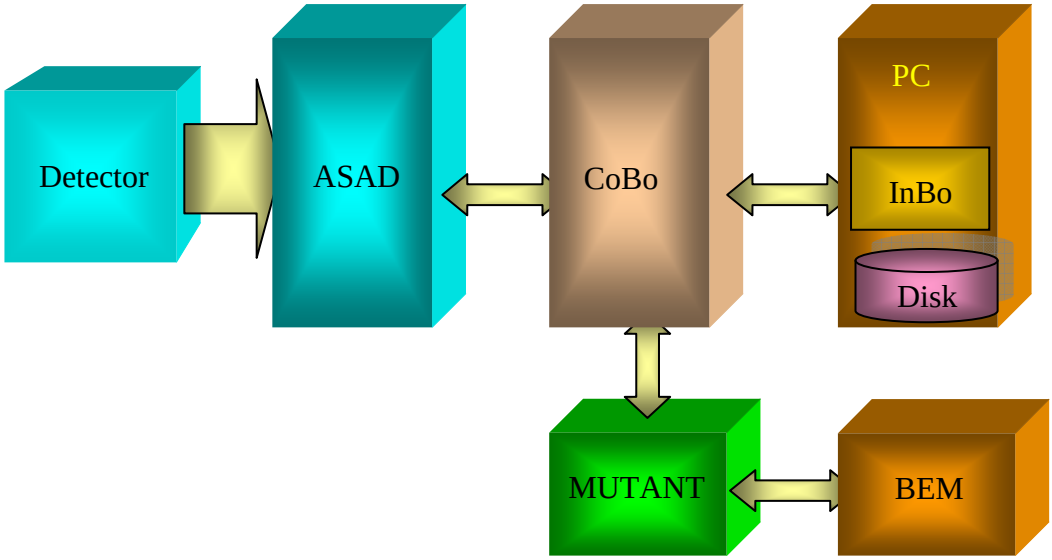
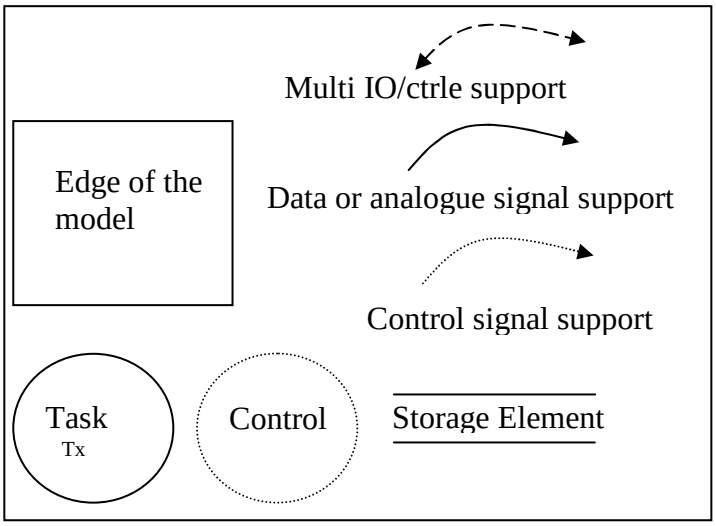


GET synoptic



Symbols legend used in this document

Chapter 1

Context

1.1 Main functions

AsAd (**As**ic-**Ad**c) board is the part of GET situated between the detector (TPC) and the digital electronics which relates with data acquisition and control processes. The main functionalities of AsAd are:

- To provide AGET (**A**SIC for **G**eneral **E**lectronics for **T**PCs) with all conditions required to make it operate properly. (T1)
- To perform the digital conversion of the analogue signals issued by the TPC and sampled by AGET (T2)
- To perform the digital conversion of the trigger sum given by AGET (T3)
- To perform the transfer of these data to **CoBo** (**CO**ncentration **Bo**ard) (T4)
- To manage its operating mode (functional, calibration and test operation) (T5)
- To deal with the slow control software system for all controls and status (T6)

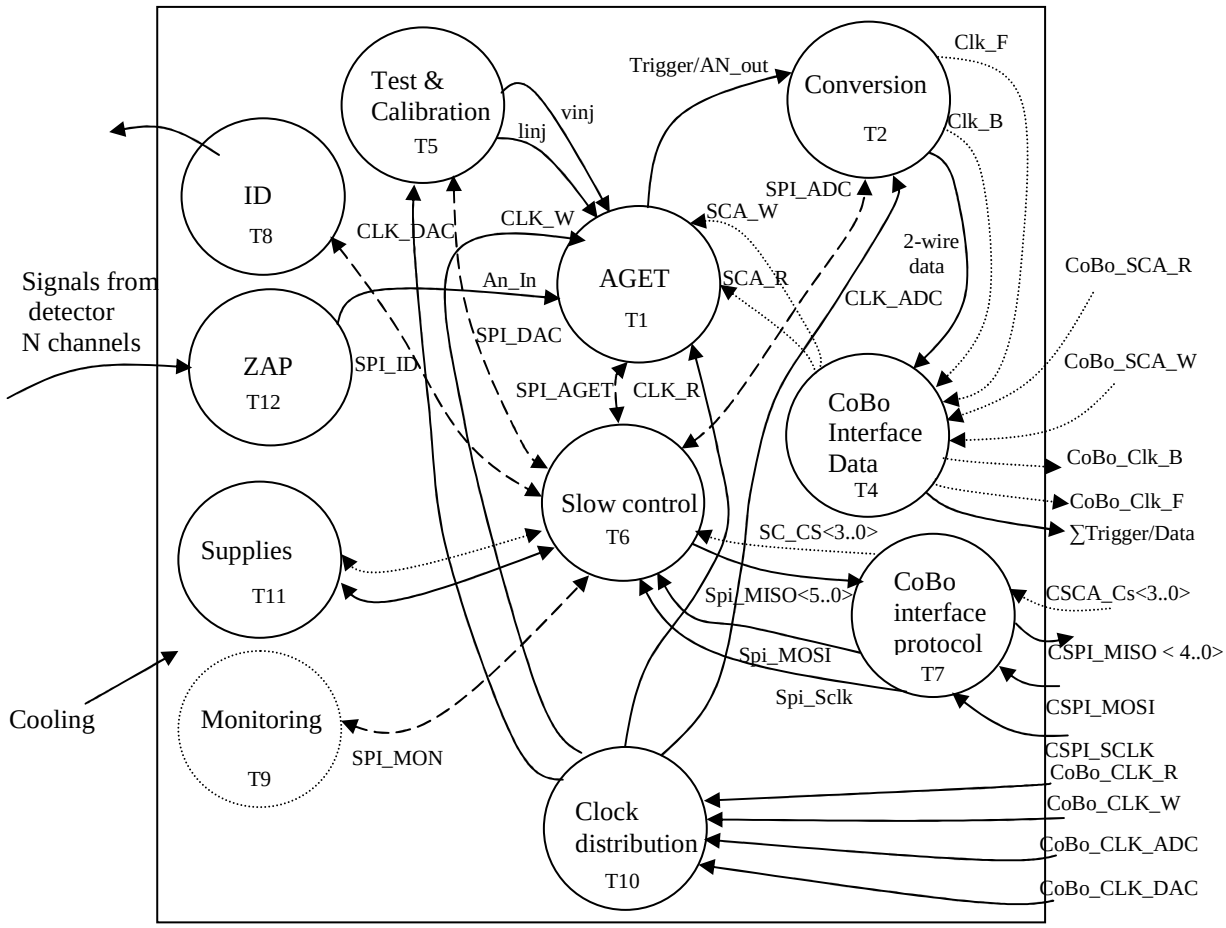


Figure 1.1: AsAd context diagram

1.2 Environmental functions

- Since all the slow control commands and status communicate with Cobo, AsAd manages its own local slow control interface (T7)
- To be identified in the whole GET systems, AsAd provides its user with ID, serial and release numbers, as well as with the type of detector connected on the system. (T8)
- AsAd enables to monitor its operating temperature and its power supply voltages/currents levels. (T9)
- AsAd manages clock signals for AGET read-write, test and calibration, slow control, analogue to digital conversion, even if CoBo is not connected on the system. (T10)
- At last AsAd manages supplies (T11) and all voltage/current biasing sources required by the components implemented in the board
- Protection against sparks from the detectors is managed by the **task ZAP** (T12).

1.3 Prototype

At this time information about MSU, CENBG and ACTAR TPC detectors lead to say that there are two major types of detectors: low density and high density. In consequence it is foreseen to build an AsAd prototype for the MSU TPC (a low density detector), which mechanical and operating environment are the best known. The following table (Table I.1) summarizes the MSU TPC specifications. This information will be used for the development of the AsAd prototypes, especially for the dimensions and the environment constraints.

Category	parameters	Value	Unit	Remark
updated: A. Bickley, June 3, 2008				
Detector Information:				
chamber type :		Cylindric		cylindric, rectangle, quarre
size:	*diameter*	**70**	cm	
	width		cm	
	length	**120**	cm	
	heigth		cm	
Readout plane		**Gem, Wire**		Gem, Micromegas, Wire chamber
Dead Zone		**4**	cm diameter	
Pad size	*length*	**5**	mm	
	width	**5**	mm	
number of Pad		**10000**		
gaz		**ALL available**		
drift speed		**200ns/cm to 2µs/cm**		
drift Time		**4µs to 50µs**	µs	
environment	*Electric Field*		V/cm	
	Magnetic Field	**0-2**	Tesla	
	Vacuum	**air**	TOR	
	Pressure	**0.2-1atm**	mBar	
	temperature	**ambiant**	°C	
	Temp. Variation	**5**	°K	
mean event rate		**100 to 1000**	Bq	Bequerel
number of touched pads/event		**1 to 25**	%	

Physics				
Type of reaction	**transfer, resonance, fission and heavy ion reactions**			
detector Gain				
Minimum ionization particles Energy				
Signal Polarity		**Pos ; Neg**		
minimum threshold		**noise level**	fC	

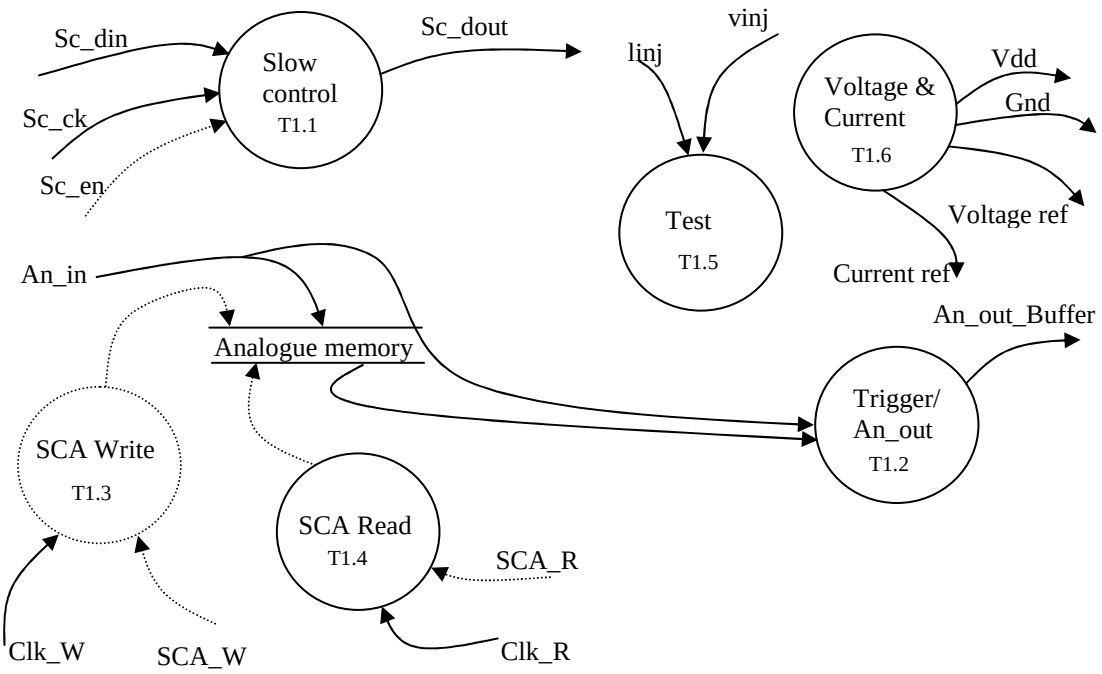
System				
Experiment Place		**MSU**		
Foreseen Acquisition		**MSU**		
Existing system		**No**		
Multiplicity		**YES**		
Trigger level		**2**		
Information type	**Waveform, Energy, Temps**			Waveform, Energy, Time
TimeStamp resolution		**10**		
Jitter		**2**		
electronic environment	**magnetic field, air**			Magnetic, Vacuum
dead Time		**< 1**	ms	

Table 1.1: MSU TPC Characteristics

Chapter 2

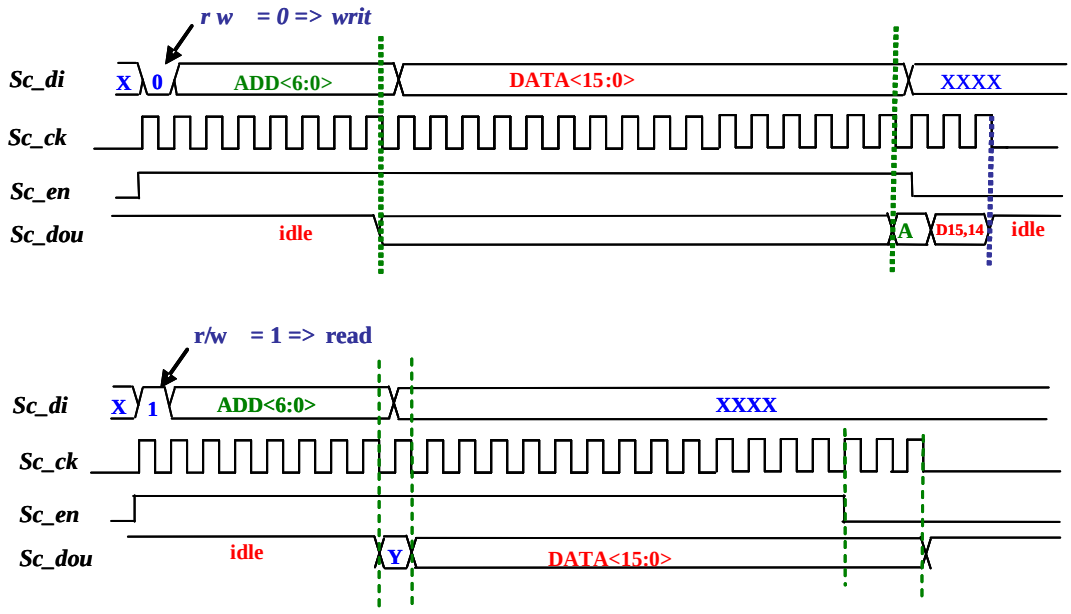
AGET Task T1

2.1 Task description



2.1.1 Slow control

Slow control is used for parameters (gain, peaking time) and hits or specific channels readout. The signals are provided by task T6. 2 modes are possible: Read OR write. 4 Signals (CMOS)



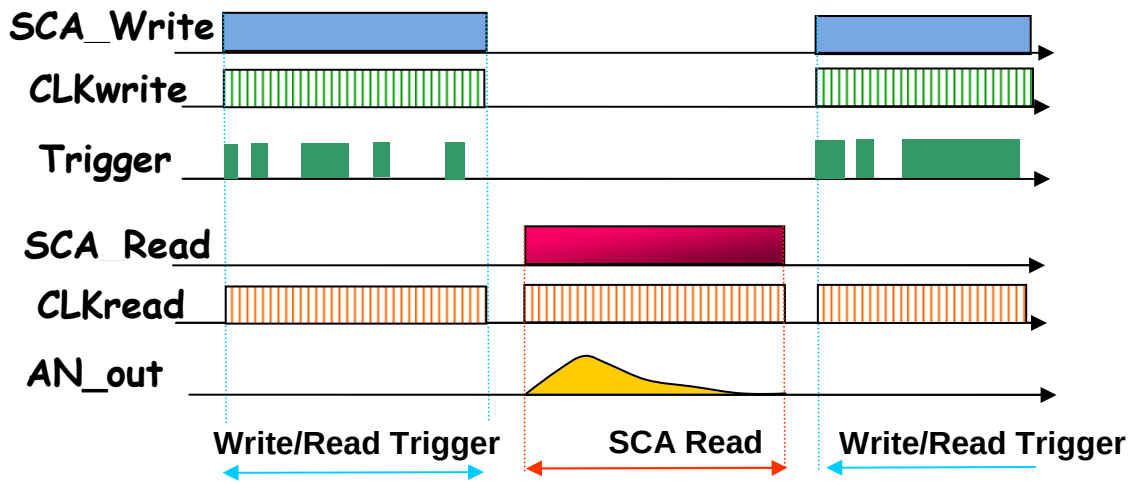
Sc_din: input data; Sc_ck: clock; Sc_en: enable; Sc_dout: output data

Name	Description	Min	Typ	Max
F Sc_ck	Slow control clock frequency	*0*		30MHz
tH_Sc_ck, tL_Sc_ck	Slow control clock minimum duration at “1” (or “0”) state	*10ns*		
t Sc_en* to *Sc_ck	delay between SC_en transition & rising edge of Sc_ck	*10ns*		
t Sc_din* to *Sc_ck	delay between SC_din transition & rising edge of Sc_ck	*10ns*		15ns
t Sc_ck* to *Sc_dout	delay between rising edge of Sc_ck & Sc_dout transition	*10ns*		

2.1.2 Trigger/AN_out

This task consists in reading the analog values stored in AGET SCA (Data extraction) as well as the sum of triggers during the sampling of the input signal (Multiplicity building).

- When the SCA is in WRITE mode the task T2 sends the analogue sum of the triggers
- When the SCA is in READ mode the task T2 sends the content of the SCA.
- The SCA READ depends of the multiplicity :
  - If the analogue sum of the triggers is equal or greater than the multiplicity, the SCA READ is launched
  - If the analogue sum of the triggers is below the multiplicity, the SCA READ is not launched.



2.1.3 SCA Write

Name	Description	Min	Typ.	Max
F *Wck*	frequency of ***Wck***	0	50MHz	100MHz
F *Wck* jitter	Jitter of ***Wck***		50 ps rms	100ps rms
F *Wck* _cycle	Duty cycle of ***Wck***	0.25	0.5	0.75
t *Wck* to Fw	Time between a ***Write*** transition and positive edge of ***Wck***	5ns		
t *Wck* to Write	Time between positive edge of ***Wck*** and a ***Write*** transition.	5ns		
t *Wck* to sample	Time between positive edge of ***Wck*** and the sample operation		3ns	

2.1.4 SCA Read

Name	Description	Min	Typ.	Max
F *Rck*	frequency of ***Rck***	0		25 MHz
***Rck* jitter**	Jitter of ***Rck***			100ps rms
***Rck* _cycle**	Duty cycle of ***Rck***	0.25	0.5	0.75
t Read to *Rck*	Time between a ***Read*** transition and positive edge of ***Rck***	5ns		
t *Rck* to Read	Time between positive edge of ***Rck*** and a ***Read*** transition.	5ns		
t *Rck* to Multiplex	Time between positive edge of ***Rck*** and the effective multiplexing		6ns	
tr multiplex	Stabilization time of the analog signal at the multiplexer output		35 ns	

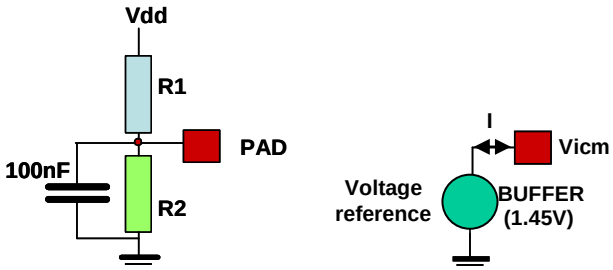
2.1.5 Test

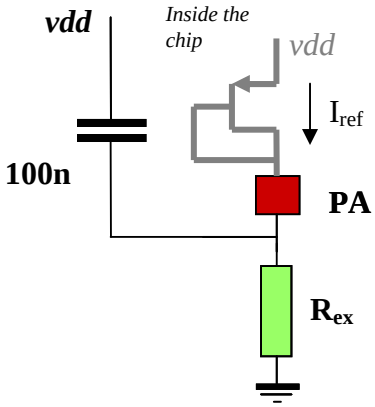
3 different modes (fixed by slow control)

- Electrical calibration : external current sent to a selected channel
- Test mode: In this mode, an external voltage signal is applied on one of the three internal injection capacitors (one capacitor per input charge range). The resulting current signal is send to the selected channel
- Functional mode: In this mode, an external voltage signal is applied on the test capacitor of the selected channel (1 channel, several channels or all channels).

2.1.6 Voltage & current

- Power supply Vdd-GND 3.3 V
- D.C voltage references:
  - CSA,Filter,G2 &SCA: 4 * 2 (left &right).
  - BUFFER: 2.





- D.C current references:
  - CSA: 1 * 2 (left &right)
  - BUFFER: 2.

- 550mW < Power consummation < 720 mW

Chapter 3

Analogue to Digital Conversion: Task T2

Under different conditions that initiate them, both multiplicity building and data encoding require an analogue to digital conversion.

3.1 Task description

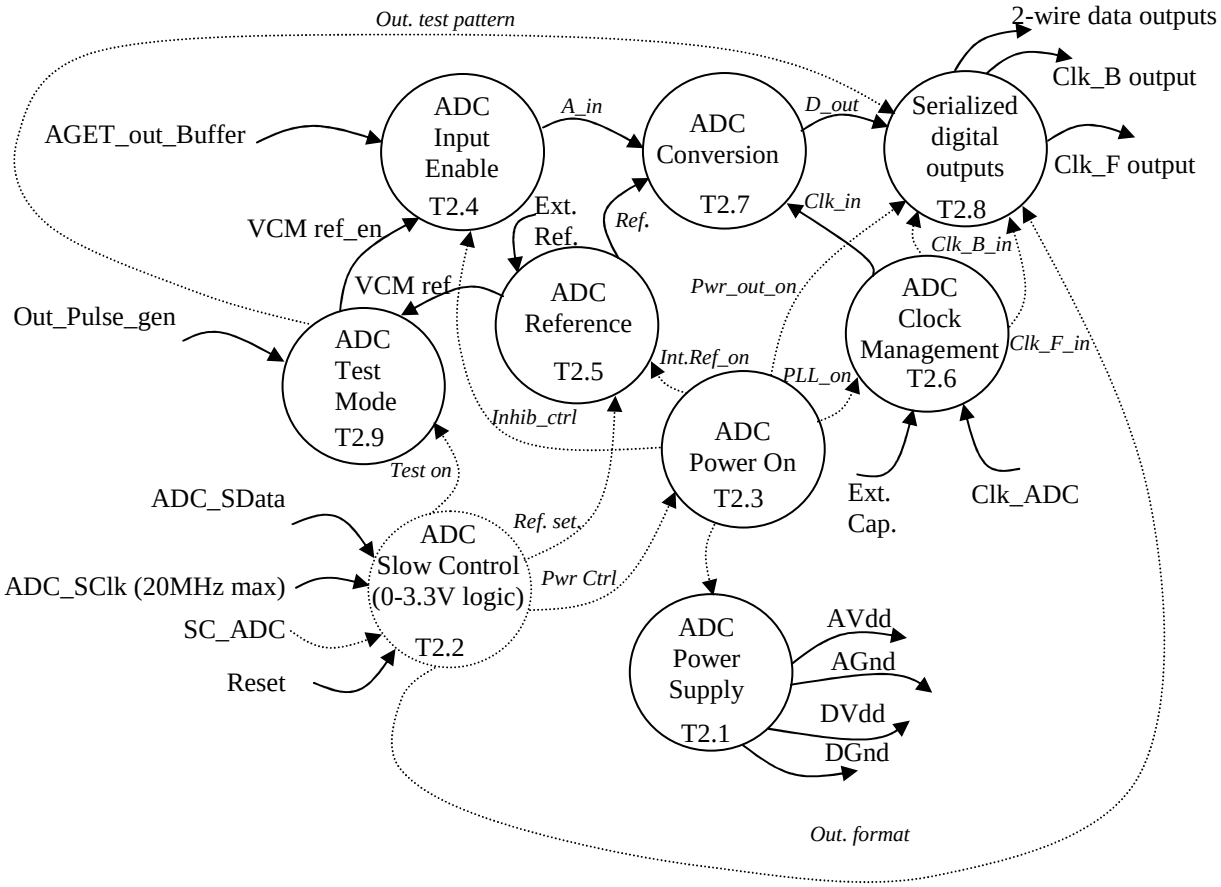


Figure 3.1: Analog to Digital conversion diagram (Based on ADS6422 datasheet)

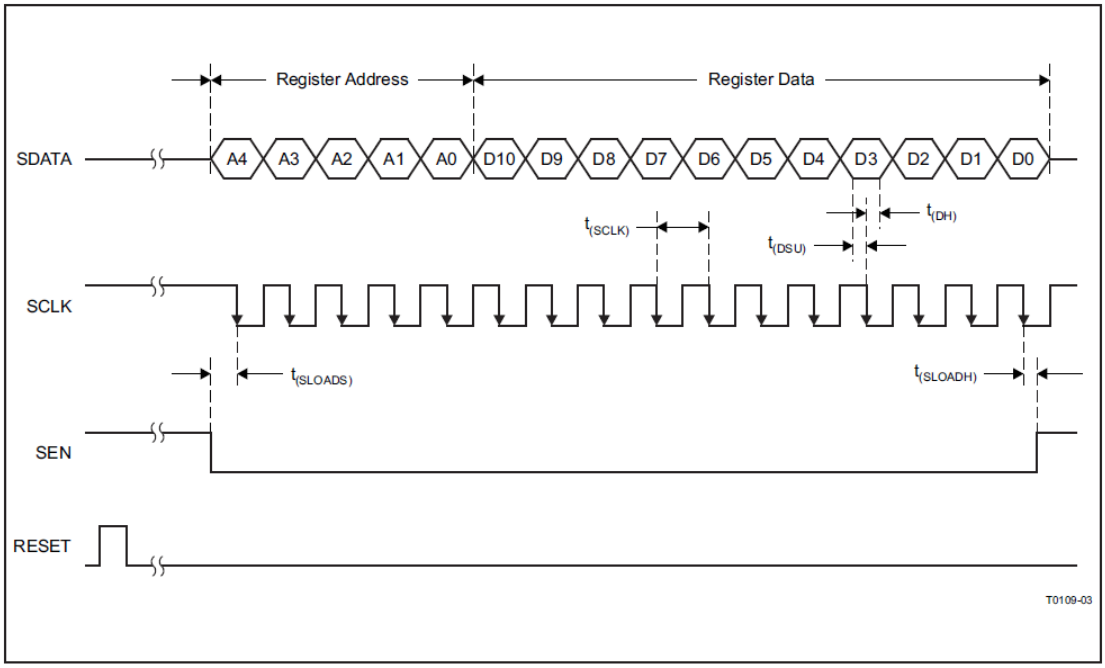
Task T2.1

AD conversion can be supplied by two 0V-3.3V power sources in order to isolate analogue processes and digital processes. These two supplies are respectively called AGnd - AVdd and DGnd -DVdd. Typical power consumption on these supplies are respectively 810mW and 250mW. A single 0V-3.3V power supply will be used with by-passing capacitors between AVdd and DVdd physical inputs.

Task T2.2

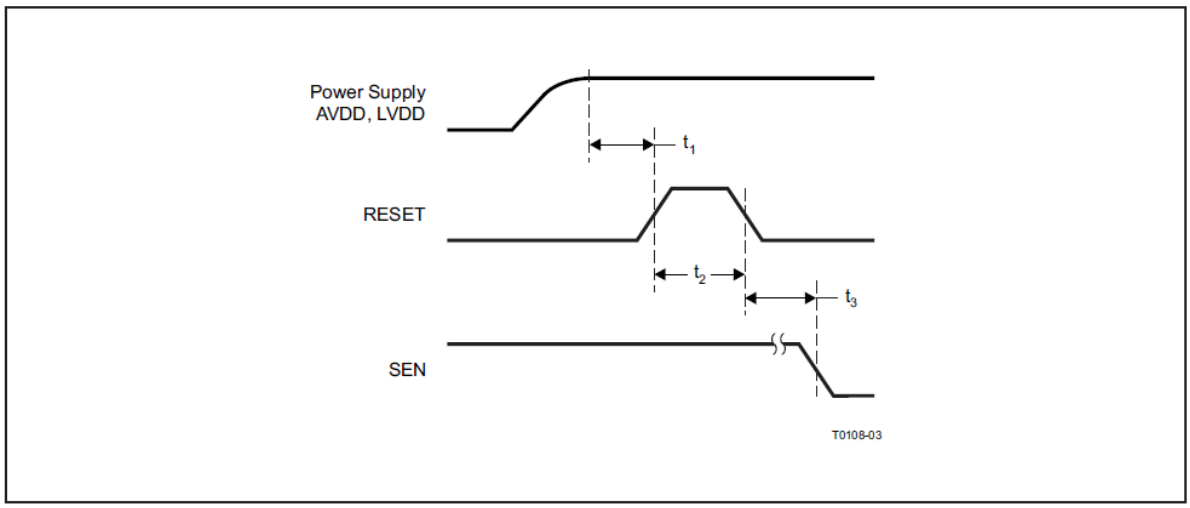
AD conversion settings are tuned by means of a serial slow control interface that deals with four signals called ADC_SData (Serial Data), ADC_SClk (Serial Clock 20MHz max), SC_ADC (or Sen, which is Chip Select) and Reset. This operating mode implies to ground the parallel interface inputs.

Eight 11-bit registers (from A to H) can be accessed to set the analogue to digital conversion process, according to the protocol represented in figure 3.2.
NB: Reset at high level brings all registers at the default values; Reset timing are given in figure 3.3



PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK Frequency, $f_{SCLK} = 1/t_{SCLK}$	> DC		20	MHz
t_{SLOADS}	SEN to SCLK Setup time		25		ns
t_{SLOADH}	SCLK to SEN Hold time		25		ns
t_{DSU}	SDATA Setup time		25		ns
t_{DH}	SDATA Hold time		25		ns
	Time taken for register write to take effect after 16th SCLK falling edge		100		ns

Figure 3.2: ADC serial interface protocol (Extracted from the ADS6422 datasheet)



PARMATER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay time	Delay from power-up of AVDD and LVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay time	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up delay time	Delay from power-up of AVDD and LVDD to output stable		6.5		ms

Figure 3.3: Reset timing (Extracted from the ADS6422 datasheet)

Tasks T2.3 & T2.4

AD conversion can be enabled or disabled by setting the power up or down, either for all channels (and all circuitry involved in the conversion process), either channel by channel according to the A-register bitmap (figure 3.4)

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	<RST> S/W RESET	0	0	0	0	<REF> INTERNAL OR EXTERNAL	<PDN CHD> POWER DOWN CH D	<PDN CHC> POWER DOWN CHC	<PDN CHB> POWER DOWN CH B	<PDN CHA> POWER DOWN CH A	<PDN> GLOBAL POWER DOWN

Figure 3.4: A-register mapping (Extracted from the ADS6422 datasheet)

D0 to D4 bits at 0 enable the conversion process by powering up all channels and associated circuitry

Task T2.5

AD conversion requires a voltage reference either internal or external. Operating with an internal voltage reference is a better choice which is authorized by leaving the D5 bit of the previous A-register at 0 (c.f. figure 3.4).
In this case the inputs common mode voltage is 1.5V and has to be matched with AGET output buffer.
E-register D10-D8 bits enable to adjust the full scale range from 1Vpp to 2Vpp (Fine gain setting) as shown in figure 3.5.
F-register D5 bit can also set the full scale range at 1.37Vpp (Coarse gain setting) as shown in figure 3.6.

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0C	<FINE GAIN> FINE GAIN CONTROL (1 dB to 6 dB)			0	0	0	0	0	0	0	<CUSTOM B> CUSTOM PATTERN (MSB BIT)

D10-D8	Full-scale range
000	0 dB Gain (full-scale range = 2.00 V_{PP})
001	1 dB Gain (full-scale range = 1.78 V_{PP})
010	2 dB Gain (full-scale range = 1.59 V_{PP})
011	3 dB Gain (full-scale range = 1.42 V_{PP})
100	4 dB Gain (full-scale range = 1.26 V_{PP})
101	5 dB Gain (full-scale range = 1.12 V_{PP})
110	6 dB Gain (full-scale range = 1.00 V_{PP})

Figure 3.5: E-register mapping (Extracted from the ADS6422 datasheet)

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0D	<OVRD> OVER-RIDE BITE	0	0	BYTE-WISE OR BIT-WISE	MSB OR LSB FIRST	<COARSE GAIN> COARSE GAIN ENABLE	FALLING OR RISING BIT CLOCK CAPTURE EDGE	0	14-BIT OR 16-BIT SERIALIZE	DDR OR SDR BIT CLOCK	1-WIRE OR 2-WIRE INTERFACE

Figure 3.6: F-register mapping (Extracted from the ADS6422 datasheet)

Tasks T2.6 & T2.7

AD conversion requires an input clock (Clk_ADC) that initiates the process at a first rising edge, on all enabled channels simultaneously.
This signal passes through an input clock buffer (figure 3.7) which gain can be adjusted according to the configuration set into the B-register (figure 3.8)

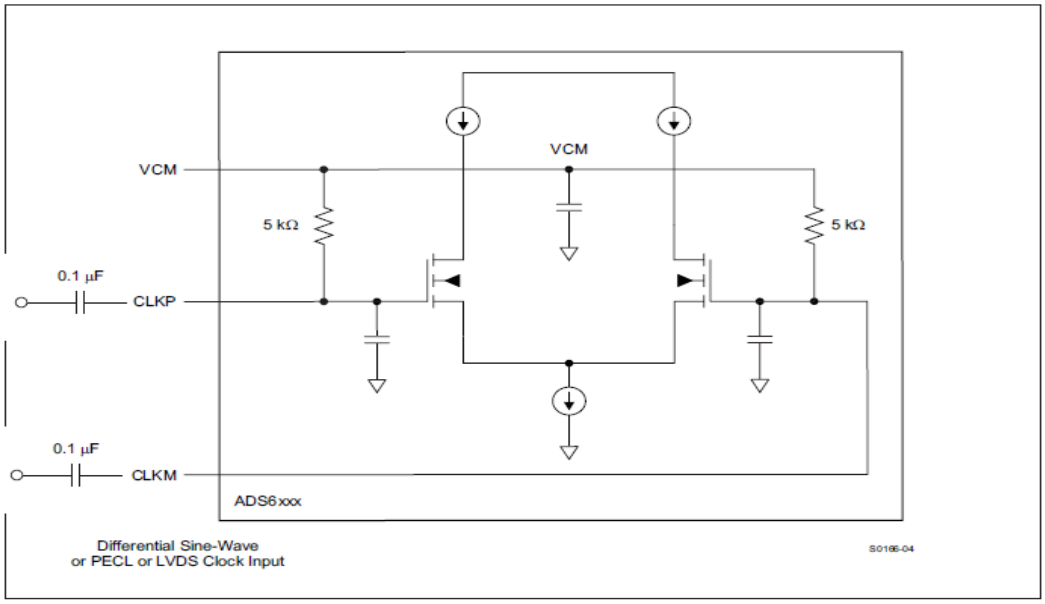


Figure 3.7: Input clock buffer (Extracted from the ADS6422 datasheet)

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
04	0	0	0	0	<CLKIN GAIN> INPUT CLOCK BUFFER GAIN CONTROL					0	0

D6-D2	Input clock buffer gain control
11000	Gain 0, minimum gain
00000	Gain 1, default gain after reset
01100	Gain 2
01010	Gain 3
01001	Gain 4
01000	Gain 5, maximum gain

Figure 3.8: B-register mapping (Extracted from the ADS6422 datasheet)

Based on this input clock, two output clock signals are generated by an internal PLL to control the unserialization of the digital outputs data. These two signals will be foreseen in T2.8 section.
NB: The PLL requires a 2nF external capacitor to work properly.

Task T2.8

The data output format can be selected by setting-up the F-register (Figure 3.6).
In order to minimize the serial data rate to transmit to CoBo, the targeted interface configuration is called "Two-wire, 12x serialization with SDR bit clock" which is selected by setting-up the F-register in this mode:
D0 at 1 (2-wire interface)
D1 at 1 (SDR bit clock)
D2 at 0 (12x serialization)
In order to make the fastest the "zero suppress" processing into CoBo, it will be convenient to discuss with CoBo designer, at the moment D6 and D7 bit can be set like this:
D6 at 1 (LSB First)
D7 at 0 (Byte wise mode)
In this configuration the data are extracted as represented in figure 3.9.
As seen in T2.7 section, the input clock (Clk_ADC) that initiates the conversion process generates two output clocks, the bit clock (Clk_B) which permits to unserialize the output data and the frame clock (Clk_F) which is aligned with the 12-bit word boundary.
The bit clock capture edge (rising in figure 3.8) can be changed by setting F-register D4 to 0
The output format previously described has to be validated by setting H-register D9 and D10 to 00 (figure 3.10)

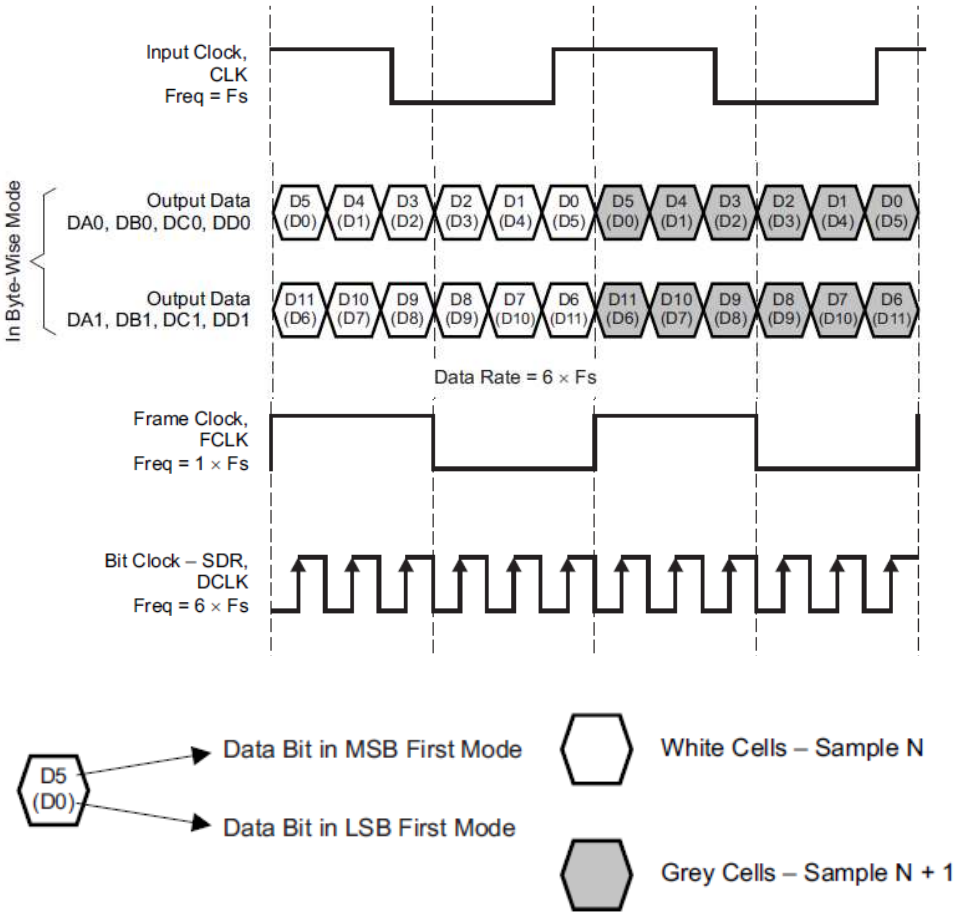


Figure 3.9: Output data format (Extracted from the ADS6422 datasheet)

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11	WORD-WISE CONTROL		0	0	0	0	<TERM DATA> LVDS INTERNAL TERMINATION - DATA OUTPUTS				

Figure 3.10: H-register mapping (Extracted from the ADS6422 datasheet)

All output logic signals are LVDS compatible. To be matched with their transmission line characteristic impedances, all output impedances can be adjusted by setting H-register D4 to D0 bits and G register D10 to D6 bits. To keep the LVDS voltage levels, all the output currents can be adjusted by setting the G register D0 to D5 bits (figure 3.11 and ADS6422 datasheet for more details)

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10	<TERM CLK> LVDS INTERNAL TERMINATION BIT AND WORD CLOCKS					<LVDS CURR> LVDS CURRENT SETTINGS				<LVDS DOUBLE> LVDS CURRENT DOUBLE	

Figure 3.11: H-register mapping (Extracted from the ADS6422 datasheet)

Task T2.9

AD conversion is an ASAD key function expected to be easily testable.
The digital part of the conversion process can be tested (task TC.9.1) separately from all the conversion process (task TC.9.2)

Task T2.9.1

C-register D7-D5 bits settings, define and supply either a predefined output data pattern (figure 3.12), either a customized output data pattern stored into D-register (11 LSB) and E-register D0 bit (1 MSB), as shown in figures 3.13 and 3.5

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	0	<DF> DATA DORMAT 2S COMP OR STRAIGHT BINARY	0	<PATTERNS> TEST PATTERNS			0	0	0	0	0

Figure 3.12: C-register mapping (Extracted from the ADS6422 datasheet)

REGISTER ADDRESS	BITS										
A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0B	<CUSTOM A> CUSTOM PATTERN (LOWER 11 BITS)										

Figure 3.13: D-register mapping (Extracted from the ADS6422 datasheet)

Task T2.9.2

In order to test all the conversion process, well known analogue signals have to be converted.

When AGET output buffer is disconnected from AGET SCA, the voltage common mode reference input, which can be viewed as a ground from a dynamic point of view, will enable to evaluate de AD conversion intrinsic noise.

By connecting AGET output buffer and applying a well known charge at AGET inputs all the signal processing chain can be checked and calibrated.

3.2 Involving context

3.2.1 SCA readout

SCA readout is initiated as soon as a trigger multiplicity has been detected.
SCA_R signal enables to start the readout process.
AGET internal multiplexor switches out the SCA output line.
Clk_R is applied to AGET and a same frequency signal, ADC_Clk, is applied to the ADC in order to control the synchronization between analogue data extraction and analogue to digital conversion.

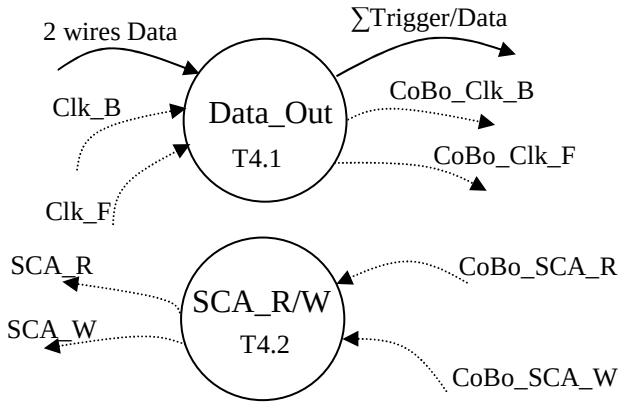
3.2.2 Multiplicity building

This task is initiated as soon as a readout cycle has been completed.
SCA_R disables the SCA readout process.
AGET internal multiplexor switches out the trigger sum output line.
Clk_R is only applied to the ADC clock input in order to build the multiplicity.
The analogue trigger sum is continuously converted to a digital code until Mutant detects the user defined multiplicity pattern.

Chapter 4

CoBo Interface Data Task T4

4.1 Task description



4.1.1 Task data_Out T4.1

This task sends to CoBo

- the digital sum of triggers during the sampling of the input signal when SCA_W is ON
- the digital values from the SCA when SCA_R is ON.
- The 2 clock signals : Clk_B to unserialize the ∑Trigger/Data and Clk_F which is aligned with the 12-bit word boundary.

since the signals are in compliance with LVDS standard, this task sets connectors and cables used for coupling to CoBo.

4.1.2 Task SCA_R/W T4.2

This task receives the SCA_R and SCA_W signals from CoBo, then sends its to the AGET task. The signals are in compliance with LVDS standard for inputs and CMOS level for outputs.

4.2 Technical part

For the Data_Out task DATA it is planned to use connectors SAMTEC QSE-DP-EM series and cables EQDP. *The availability of cables 2 meters in length must be checked*. The same connector will be used for the 2 CMOS signals from the task SCA_R/W.

- QSE main characteristics:Differential Pair, 8.5 GHz / 17 Gbps.

Crosstalk

In pin out descriptions, "G" represents terminals tied to ground, as is the ground plane. For differential measurements, "D1" and "D2" represent driven pair terminals, and "M1" and "M2" represent measured pair terminals.

Worst Case Differential Crosstalk Across Ground Plane

G	D1	D2	G
G	M1	M2	G

	Crosstalk (%)						
Signal Rise time	30 ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	undetectable	undetectable	undetectable	undetectable	undetectable	undetectable	undetectable
FEXT	undetectable	undetectable	undetectable	undetectable	undetectable	undetectable	undetectable

Worst Case Differential Crosstalk on One Side of Ground Plane

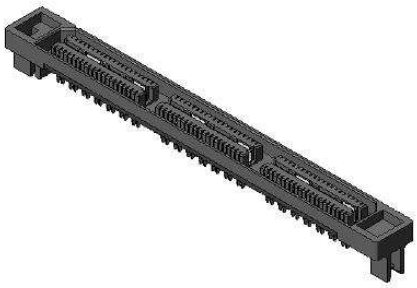
G	D1	D2	M1	M2	G

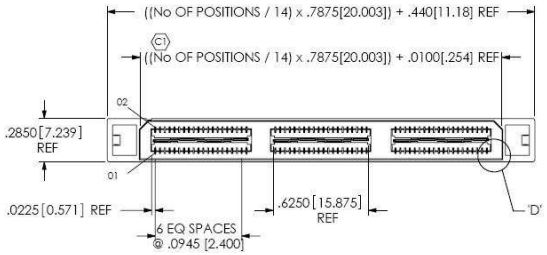
	Crosstalk (%)						
Signal Rise time	30 ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	3.7	3.6	3.2	1.8	1.0	0.7	0.5
FEXT	1.97	1.46	0.91	0.41	0.23	0.16	0.11

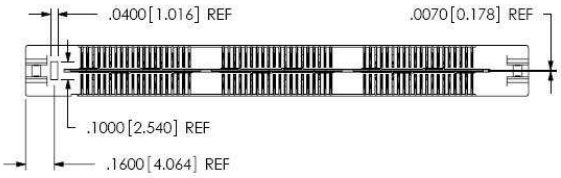
Best Case Differential Crosstalk on One Side of Ground Plane

G	D1	D2	G	M1	M2	G

	Crosstalk (%)						
Signal Rise time	30 ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	0.5	0.4	0.3	0.2	0.11	0.065	0.064
FEXT	1.44	0.99	0.70	0.33	0.15	0.11	0.07





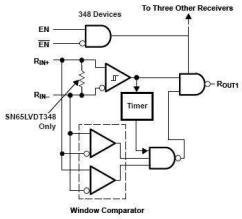


- LVDS receivers for SCA_R and SCA_W : SN65LVDS348
  - The -4 V to 5 V common-mode range allows usage in harsh operating environments or accepts LVPECL,PECL, LVECL, ECL, CMOS, and LVCMOS levels without level shifting circuitry

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	2.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, failsafe disable time				12	ns
t_{d2}	Delay time, failsafe enable time		0.3		1.5	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL1} - t_{pLH1} \rvert$)			200		ps
$t_{sk(o)}$	Output skew(2)			150		ps
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_r	Output signal rise time			1.2		ns
t_f	Output signal fall time			1		ns
t_r	Output signal rise time	C_L = 1 pF, See Figure 3		650		ps
t_f	Output signal fall time			400		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4 and Figure 5		5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5	9	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8	12	ns



Chapter 5

Test & Calibration: Task T5

Introduction

AGET main functions have to be easily testable.
AGET test & calibration consist in injecting a well known charge quantity at its inputs to test the channel responses and to evaluate precisely the signal processing features (c.f. figure 5.1).

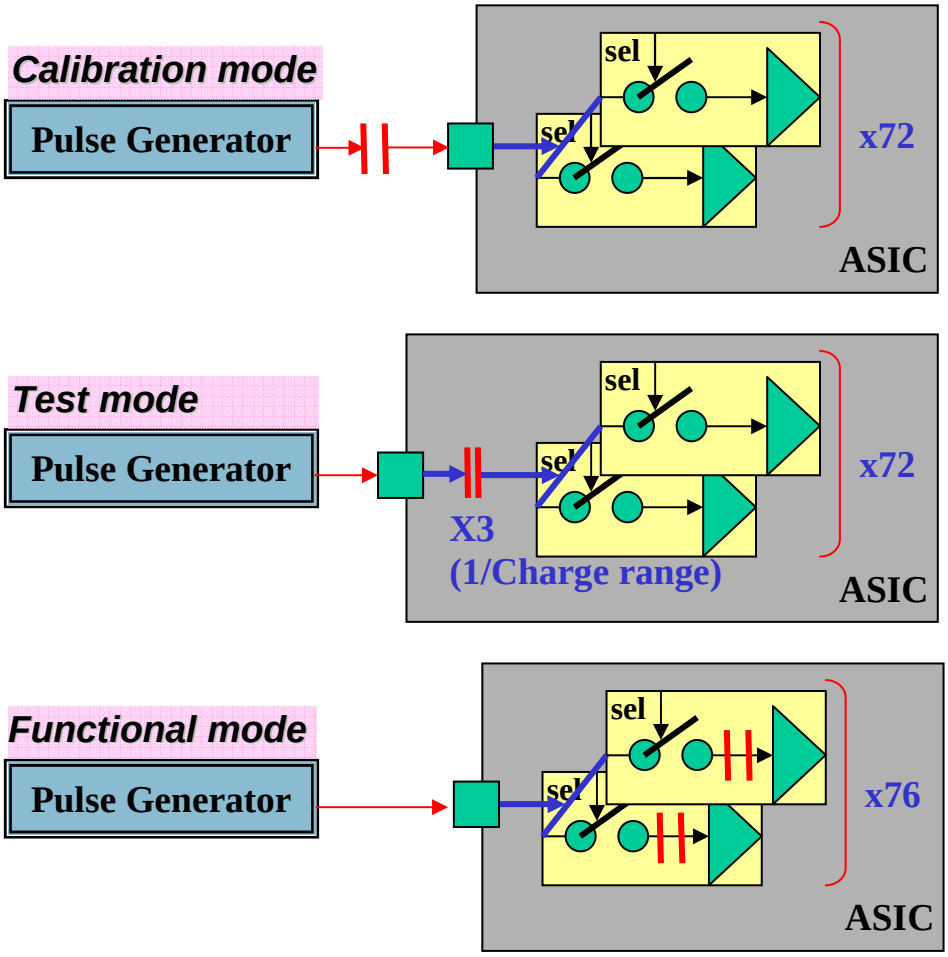


Figure 5.1: AGET operating modes (Extracted from AGET specification)

These operating modes require a voltage generator which output value can sweep all AGET input dynamic range (according to AGET specifications, input noise level σ is around 850 e- i.e. ≈ 0.14 fC, in optimal case, and linear operation is preserved until 10pC). Assuming a SNR at least equal to 5σ, the voltage output dynamics must be greater than 14.10^3. As the voltage generator has to be remote controlled, it will be made of a 14-bit DAC (Digital to Analog Converter).
The DAC main feature in this application is its linearity. With both DC and AC high linearity features the AD9707 is a good choice to meet the requirements in test and calibration

5.1 Task description

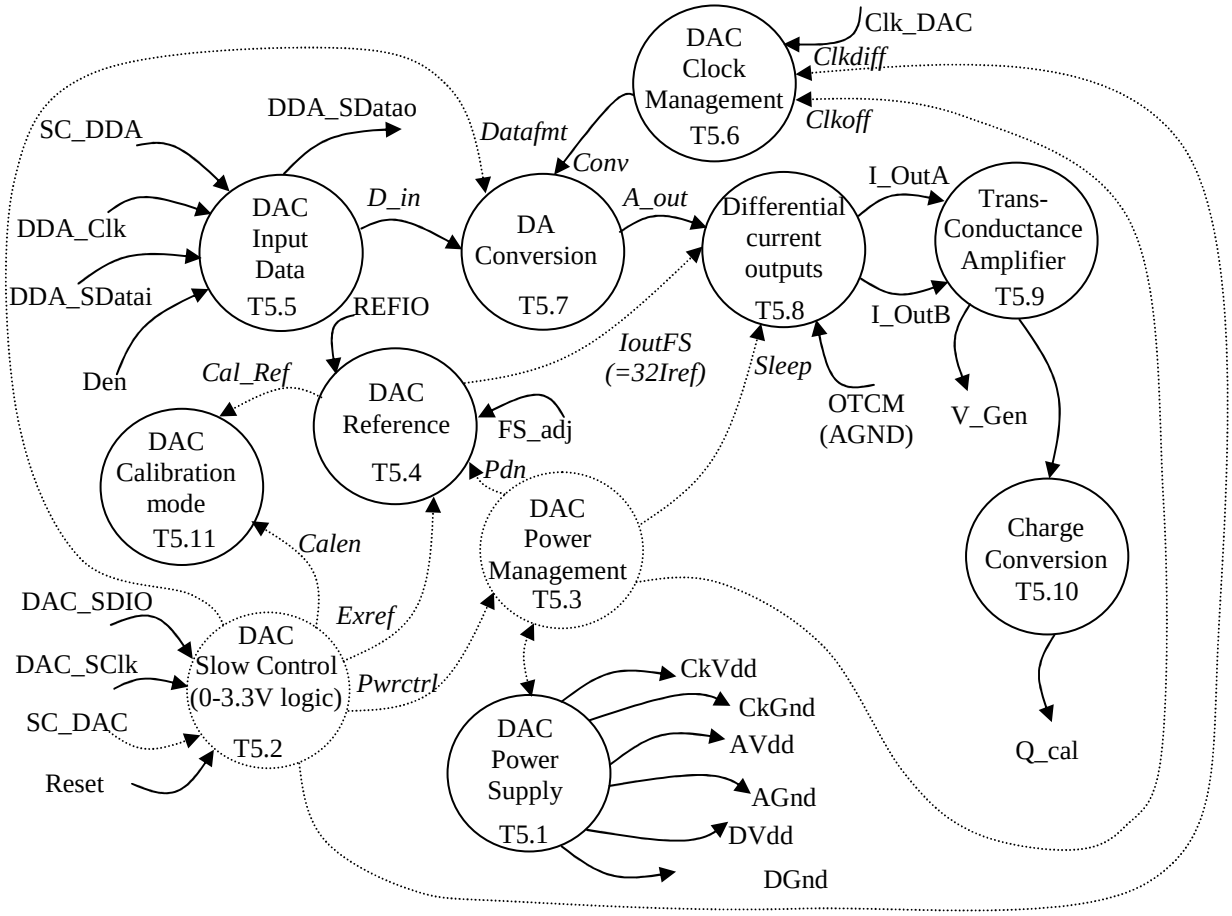


Figure 5.2: Analog to digital conversion diagram (Mainly based on AD9707 datasheet)

Task T5.1

DA conversion requires three 0V-3.3V power supplies in order to isolate analogue, digital and clocking processes. These three supplies are respectively called AGnd – AVdd, DGnd – DVdd, CkGnd – CkVdd. Maximal power consumptions on these supplies are respectively 23mW, 22mW and 16mW. A single 0V-3.3V power supply will be used with by-passing capacitors between AVdd, DVdd and CkVdd physical inputs.

Task T5.2

DA conversion settings are tuned by means of a SPI slow control interface that deals with four signals called DAC_SDIO (Serial Data Input/Output), DAC_SClk (Serial Clock 20MHz max), SC_DAC (Chip Select) and Reset (logic high to low transition cancels any SPI instruction).
Eight 8-bit registers can be accessed to set the digital to analogue conversion process. Each data transfer cycle follows an instruction cycle in which the MSB value indicates whether a read or write operation (0 for write, 1 for read), the two following bits indicates the number of bytes to be transferred (1 to 4; 2 bytes preferred corresponds with code 01), and the 5 last bits (including the LSB) determines the register address to be accessed.
Serial port configuration itself is controlled by the SPI _ctrl register first 4 bits (Figure 5.3)

Mnemonic	Bit No.	Direction (I/O)	Default	Description
SDIODIR	7	I	1	0: SDIO pin configured for input only during data transfer (4-wire interface). 1: SDIO pin configured for input or output during data transfer (3-wire interface).
DATADIR	6	I	0	0: Serial data uses MSB first format. 1: Serial data uses LSB first format.
SWRST	5	I	0	1: Initiate a software reset; this bit is set to 0 upon reset completion.
LNGINS	4	I	0	0: Use 1 byte preamble (5 address bits). 1: Use 2 byte preamble (13 address bits).
PDN	3	I	0	1: Shuts down DAC output current internal band gap reference.
SLEEP	2	I	0	1: DAC output current off.
CLKOFF	1	I	0	1: Disables internal master clock.
EXREF	0	I	0	0: Internal band gap reference. 1: External reference.

Figure 5.3: SPI_ctrl register @ address 0x00 (Extracted from AD9707 datasheet)

Default configuration for SDIODIR, DATADIR, SWRST and LNGINS bits (figure 5.3) will be kept.
In this configuration the SPI interface timing is given in figure 5.4.

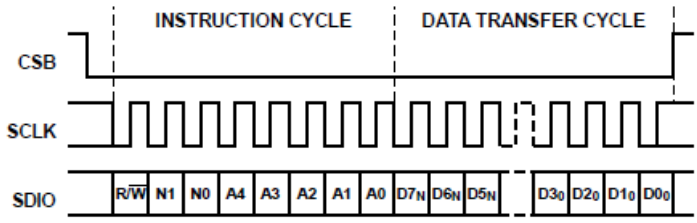


Figure 5.4.1: SPI interface timing in writing mode (N=1)

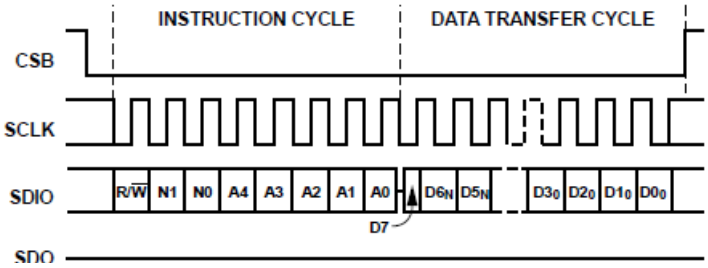


Figure 5.4.2: SPI interface timing in reading mode (N=1)

Figure 5.4: SPI interface timing(Extracted from AD9707 datasheet)

Task T5.3

The PDN, SLEEP, CLKOFF bits configuration of the previously described SPI_ctrl register enable all the DA conversion process by default (default code is 000).
Anyway, whether the internal reference, the output current buffer or the input clock buffer power supplies can be switched off when no DA conversion is required (i.e. when ASAD is not operated in test or calibration mode).

Task T5.4

The EXREF bit value of the previously described SPI_ctrl register (LSB) determines whether the use of an external reference voltage or the use of the internal 1V band gap voltage reference. The default configuration (use of the internal band gap reference) will be kept.
NB: In this configuration RFIO has to be bypassed to ground with a 0.1µF capacitor
The 1V band gap voltage reference together with an external resistor determines a static reference current Iref which is equal to the full scale reference current output IoutFS. IoutFS equal to 1mA (the lower admissible value in order to limit the power consumption) implies

Iref equal to 31.25 μA. From the 1V band gap reference, Iref is generated using a ground connected 32kΩ resistor to the FS_adj input.

Task T5.5

The digital input code is transferred to ASAD using a serial protocol that deals with four signals called DDA_SDatai (Data serial input), DDA_SClk (Data serial clock), SC_DDA (Chip Select) and DDA_SDatao (Data serial output).
As the AD9707 is a parallel data input DAC, the digital input code is deserialized by means of two cascaded 8-bit shift registers (for example SN74LV595AD from TI or 74LVC595A from NXP).
DDA_SDatai is then a 16-bit word with a MSB value always equal to 1, which contains on the last 14 bits, the DAC data input.
DDA_SClk is the common slow control clock that initiates the shift operation.
SC_DDA is the shift registers clear control that is used to enable the shift operation.
DDA_SDatao is a signal sent to the slow control to indicate that the Dac data input is ready to be loaded.
From DDA_SDatao signal, CoBo supplies Den which load the data at the DAC parallel input.
All these operations are summarized in figure 5.5

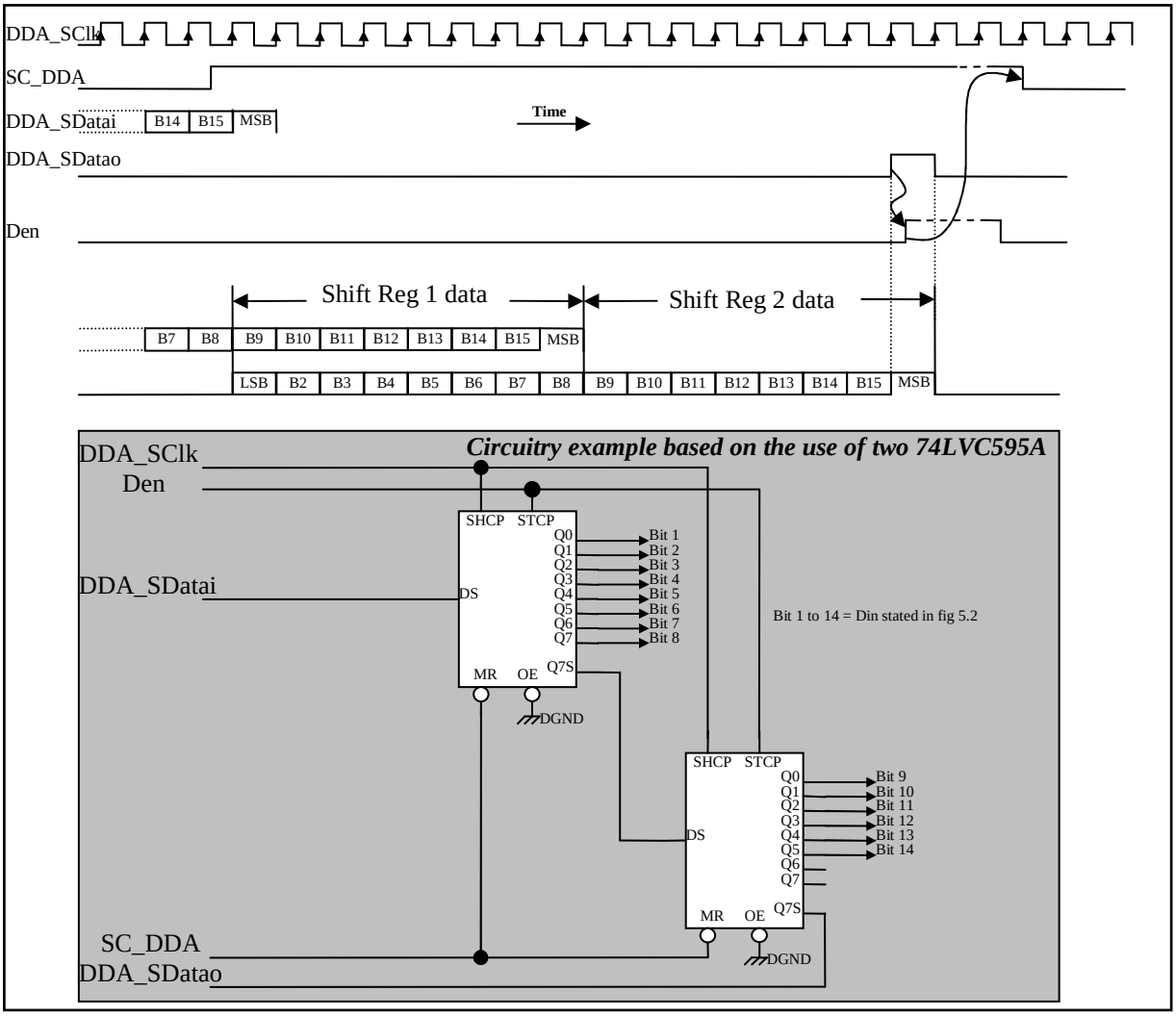


Figure 5.5: DAC input data loading (timing & circuitry diagrams)

Task T5.6

The input clock signal that initiates the DA conversion passes through an internal buffer which can be powered off as mentioned in section task T5.3.
When enabled, the clock input has to be configured to receive a single ended or a differential signal. This is achieved by setting the value of the CLKDIFF bit (bit 2) of the Data-Register (address 0x02), as illustrated in figure 5.6

Mnemonic	Bit No.	Direction (I/O)	Default	Description
DATAFMT	7	I	0	0: Unsigned binary input data format. 1: Twos complement input data format.
DCLKPOL	4	I	0	0: Data latched on DATACLK rising edge always. 1: Data latched on DATACLK falling edge (only active in DESKEW mode).
DESKEW	3	I	0	0: DESKEW mode disabled. 1: DESKEW mode enabled (adds a register in digital data path to remove skew in received data; one clock cycle of latency is introduced).
CLKDIFF	2	I	0	0: Single-ended clock input. 1: Differential clock input.
CALCLK	0	I	0	0: Calibration clock disabled. 1: Calibration clock enabled.

Figure 5.6: Data register @ address 0x02 (Extracted from AD9707 datasheet)

A differential clock is preferred CLKDIFF bit keeps the 0 default value. The clock signal applied must have a common mode voltage comprised between 0.75V and 2.25V and a differential value comprised between 0.5V and 1.5V (LVPECL levels compatible).
The DA conversion is initiated at the positive signal rising edge.
NB: At this moment the parallel input data must be present at the shift registers outputs described in section Task 5.5. Then the clock rising edge must be emitted after the Den signal

Task T5.7

DA conversion process is parameterized by choosing the bit values of the previously seen Data register (Figure 5.6)
DATAFMT is left at the 0 default value to convert the loaded DAC unsigned binary input data.
DCLKPOL is also left at the 0 default value to initiate the DA conversion on the Clk_DAC rising edge. No deskew is required to perform the task, DESKEW bit is then left at default value.

Task T5.8

Output currents Iout_A and Iout_B are respectively given by:

$$IOUTA = (DAC\ CODE/2^N) \times I_{OUTFS}$$

$$IOUTB = ((2^N - 1) - DAC\ CODE)/2^N \times I_{OUTFS}$$

With IoutFS equal to 1mA (see section T5.4) and N=14

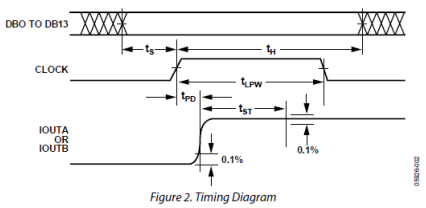


Figure 2. Timing Diagram

Figure 5.7: Conversion timing (Extracted from AD9707 datasheet)

Output current is supplied at least 15ns after the DAC clock rising edge (figure 5.7 with ts_ min= 1.6 ns, tpd _min=4ns, tst_min=11ns, tlpw_min=2.8ns)
Full scale current supplies a max 1 V output voltage sweep, by connecting a resistor on each output Iout_A and Iout_B (OTCM has to be also ground connected in this configuration)

Task T5.9

The pulse generator required for test & calibration supplies V_GEN voltage by loading the DAC current outputs with the circuit represented in figure 5.8

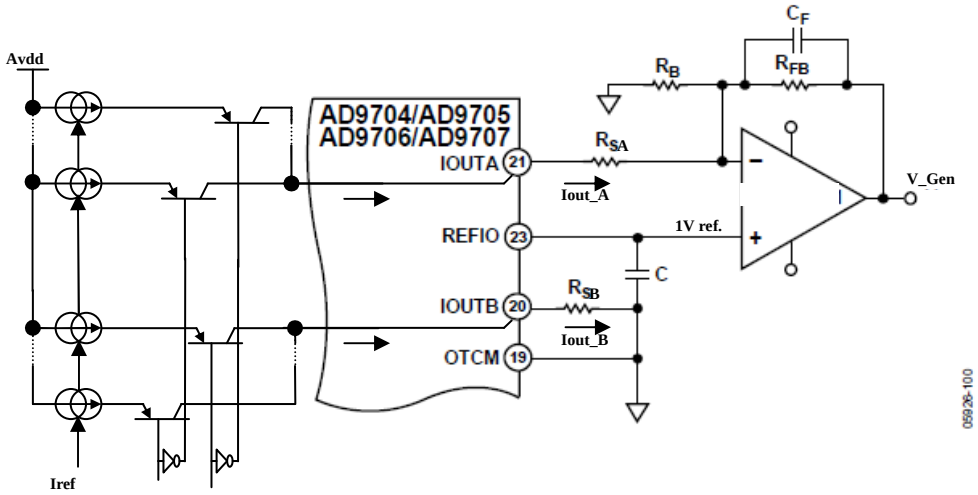


Figure 5.7: Transconductance amplifier (Partly extracted from AD9707 datasheet)

$Iout\_A_{max}$= 1mA when $Iout\_B_{min}$= 0 mA
Voltage drop across R_{SA} =1kΩ is 1V and VAout_A is then equal to VAout_B=0V
$Iout\_A_{min}$= 0 mA when $Iout\_B_{max}$= 1 mA
Voltage drop across R_{SB} =1kΩ is 1V and VAout_B is then equal to VAout_A=1V
At mid range of the full-scale output current VAout_A and VAout_B are both equal to 0.5V
DAC output voltage ranges are then ±0.5V from 0.5V
R_B and R_{FB} both equal to 2kΩ sets the max voltage V_Gen equal to 2V when Iout_A= 0 and the min voltage V_Gen equal to 0V when Iout_A= 1mA
V_Gen has to be whether send out of ASAD (to evaluate DAC performances) or applied to AGET In_testfonc input pin (figure 5.8)

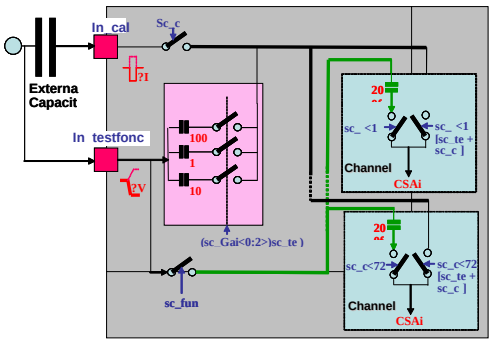


Figure 5.8: AGET connections for test & calibration modes (Extracted from AGET specifications)

Task T5.10

Charge conversion is achieved by the external capacitor represented in figure 5.8. The tolerance value of this capacitor is as low as possible. The charge is injected at the AGET In_cal input pin.

Task T5.11

To improve the DNL of the DA converter a self-calibration procedure can be carried out according to the procedure described in figure 5.9

The calibration clock frequency is equal to the DAC clock divided by the division factor chosen by the DIVSEL value. The frequency of the calibration clock must be set to under 10 MHz for reliable calibrations. Best results are obtained by setting DIVSEL[2:0] (Register 0x0E, Bit 2 to Bit 0) to produce the lowest frequency calibration clock frequency that the user's system requirements allow.

To perform a device self-calibration, the following procedure can be used.

1. Enable the calibration clock by setting the CALCLK bit (Register 0x02, Bit 0).
2. Enable self-calibration by writing 0x40 to Register 0x0F.
3. Wait approximately 4500 calibration clock cycles. Each calibration clock cycle is between 2 and 256 DAC clock cycles, depending on the value of DIVSEL[2:0].
4. Check if the self-calibration has completed by reading the CALSTAT bit (Register 0x0F, Bit 7). A Logic 1 indicates the calibration has completed.
5. When the self-calibration has completed, write 0x00 to Register 0x0F.
6. Disable the calibration clock by clearing the CALCLK Bit (Register 0x02, Bit 0).

The AD9704/AD9705/AD9706/AD9707 devices allow reading and writing of the calibration coefficients. There are 33 coefficients in total. The read/write feature of the coefficients can be useful for improving the results of the self-calibration routine by averaging the results of several calibration results and loading the averaged results back into the device. The reading and writing routines follow.

To read the calibration coefficients:

1. Enable the calibration clock by setting the CALCLK bit (Register 0x02, Bit 0).
2. Write the address of the first coefficient (0x00) to Register 0x10.
3. Set the SMEMRD bit (Register 0x0F, Bit 2) by writing 0x04 to Register 0x0F.
4. Read the value of the first coefficient by reading the contents of Register 0x11.
5. Clear the SMEMRD bit by writing 0x00 to Register 0x0F.
6. Repeat Step 2 through Step 5 for each of the remaining 32 coefficients by incrementing the address by one for each read.
7. Disable the calibration clock by clearing the CALCLK Bit (Register 0x02, Bit 0).

To write the calibration coefficients to the device:

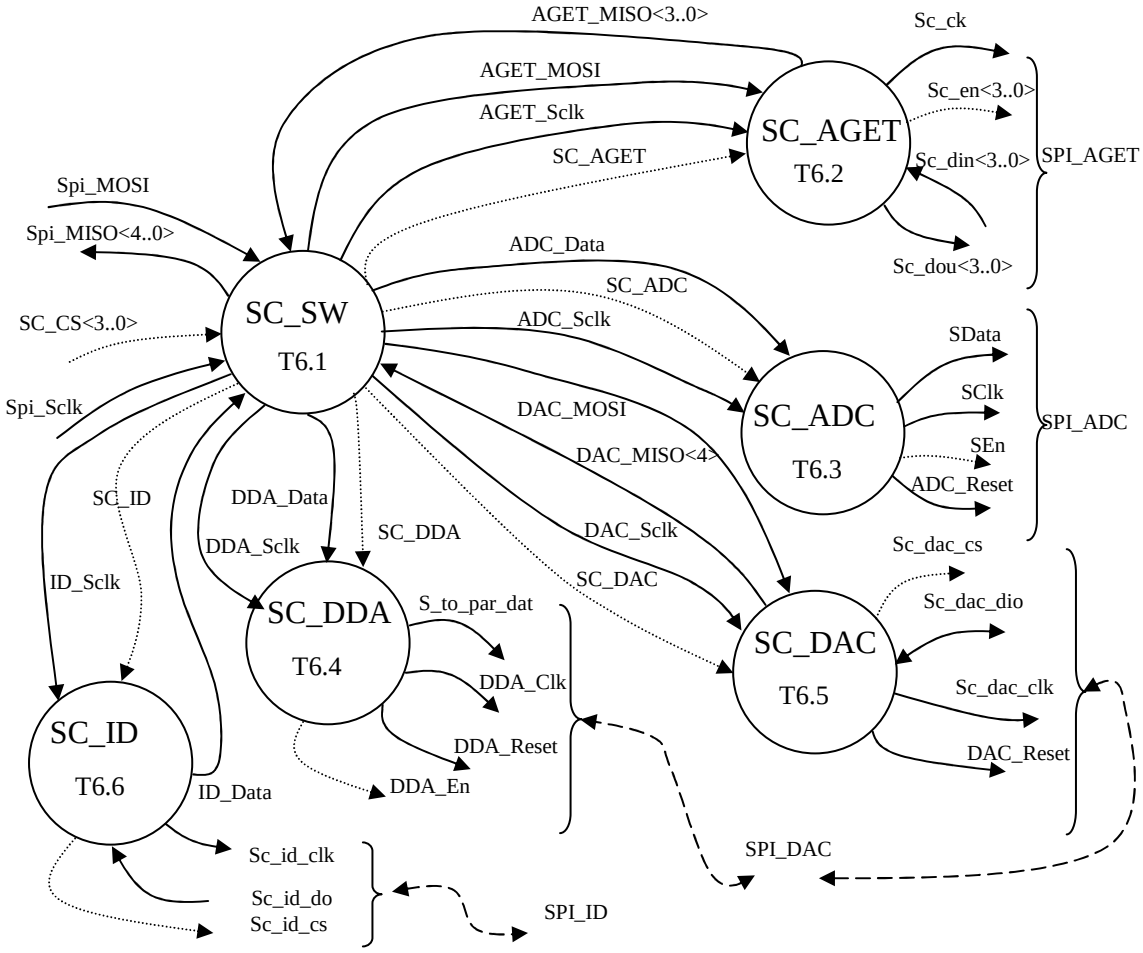
1. Enable the calibration clock by setting the CALCLK bit (Register 0x02, Bit 0).
2. Set the SMEMWR bit (Register 0x0F, Bit 3) by writing 0x08 to Register 0x0F.
3. Write the address of the first coefficient (0x00) to Register 0x10.
4. Write the value of the first coefficient to Register 0x11.
5. Repeat Step 2 and Step 3 for each of the remaining 32 coefficients by incrementing the address by one for each write.
6. Clear the SMEMWR bit by writing 0x00 to Register 0x0F.
7. Disable the calibration clock by clearing the CALCLK bit (Register 0x02, Bit 0).

Figure 5.9: DAC self-calibration procedure (Extracted from AD9707 datasheet)

Chapter 6

Slow Control Task T6

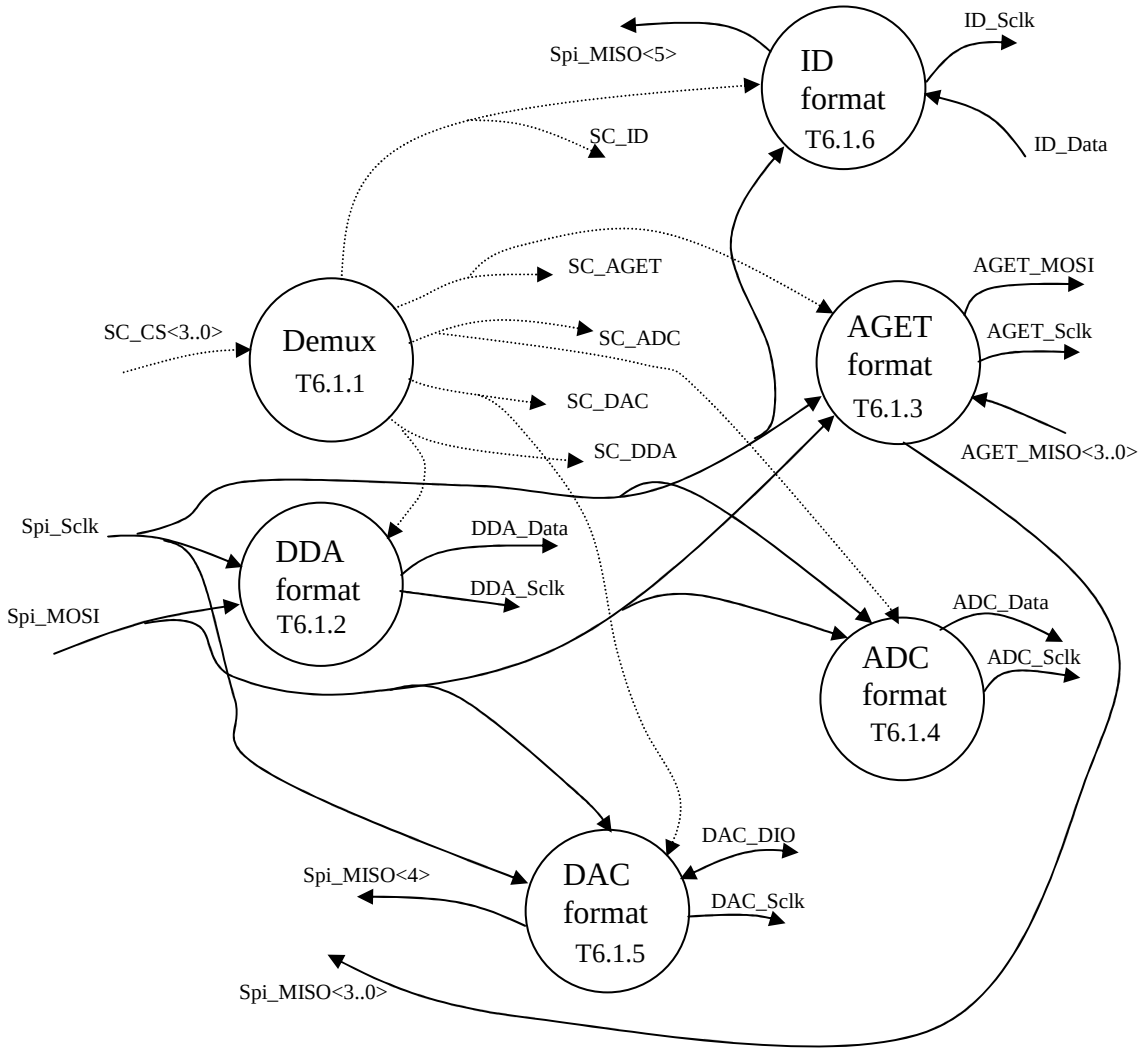
6.1 Task description



6.1.1 Summary of the pattern of slow control

Device	Clock freq	Add size (bit)	Data size (bit)	Level (V)	First bit I/O
SC_AGET	0 < ckl <30 MHz	7 +1 R/W	16	3.3	D15
SC_ADC	0 < ckl <20 MHz	5	11	3.3	D10
SC_DAC	0 < ckl <20 MHz	5+1 R/W +2 dat size	16	3.3	D15
SC_DDA	0 < clk <90 MHz	0	16	3.3	D15
SC_ID	0 <clk < 30 MHZ	1	16	3.3	D15

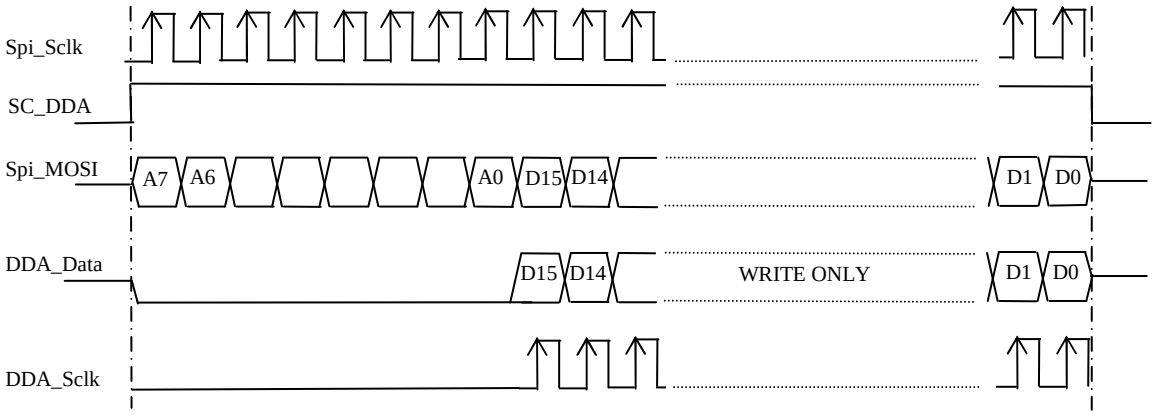
6.1.2 Slow control switcher task T6.1



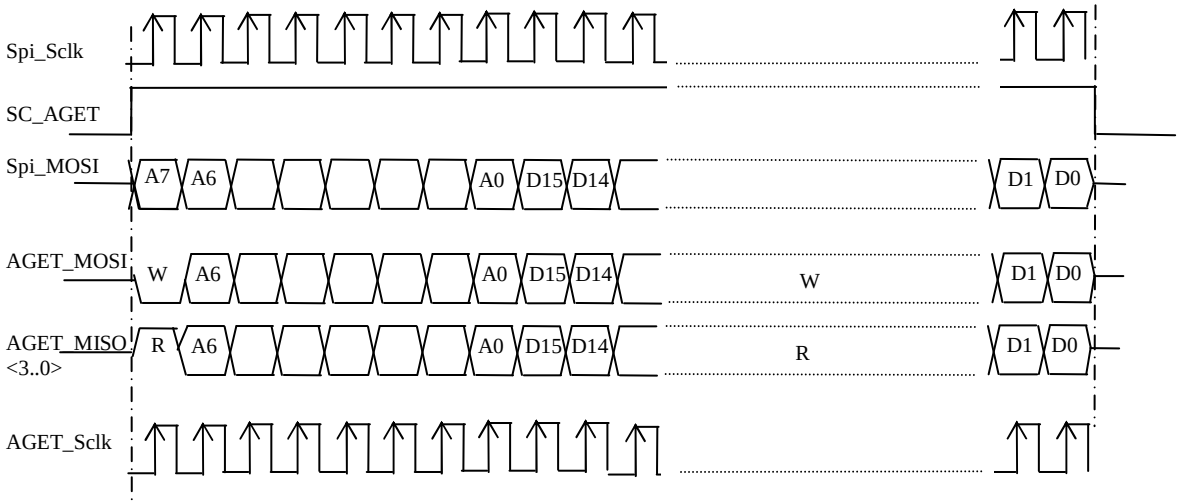
6.1.2.1 Demux task T6.1.1

Demux 4 to 15 to select the right SPI address format

6.1.2.2 Serial to parallel converter for DAC task T6.1.2

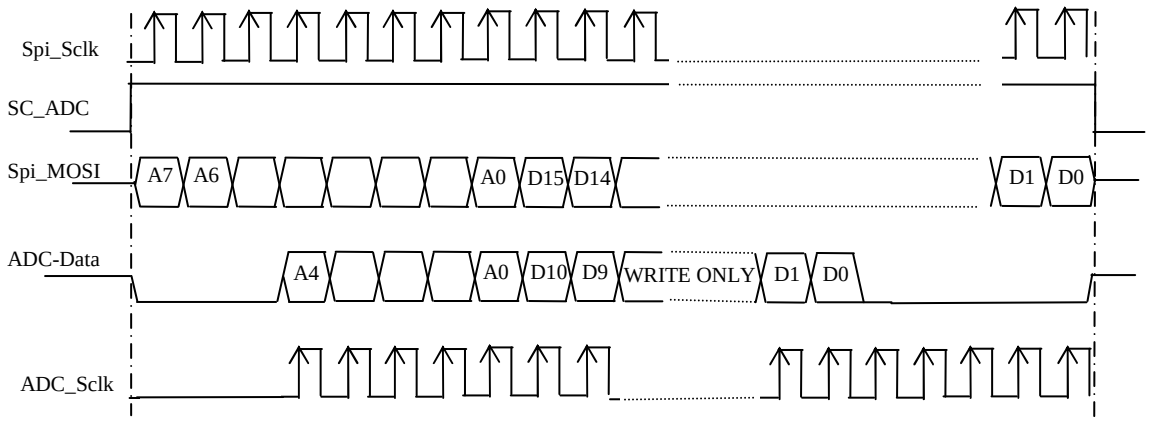


6.1.2.3 AGET Address and Data format task T6.1.3

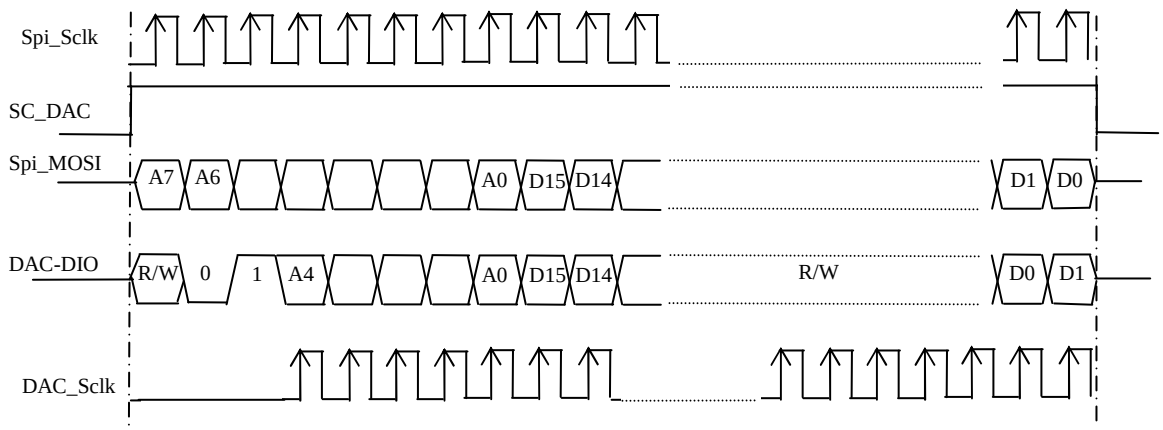


Hit channel register readout: 4.5 µs/AGET

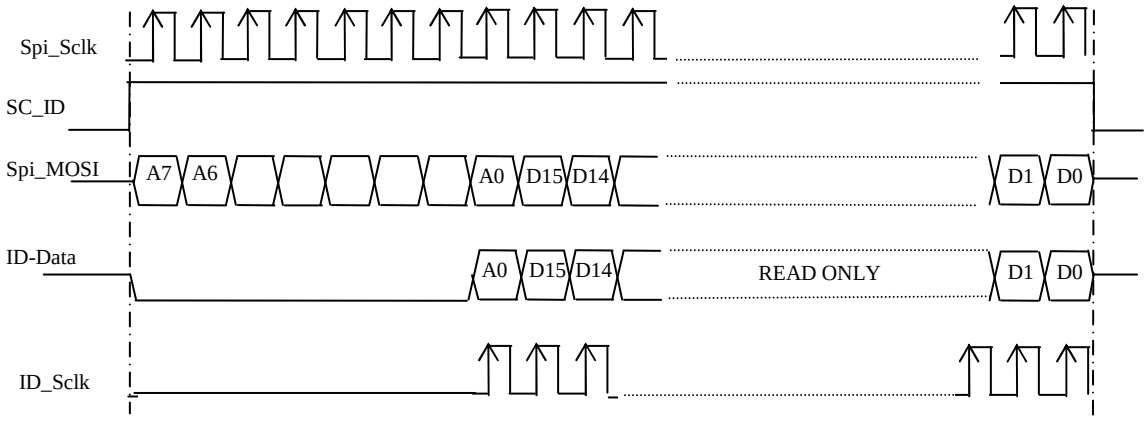
6.1.2.4 ADC Address and Data format task T6.1.4



6.1.2.5 DAC Address and Data format task T6.1.5



6.1.2.6 ID Address and Data format task T6.1.6

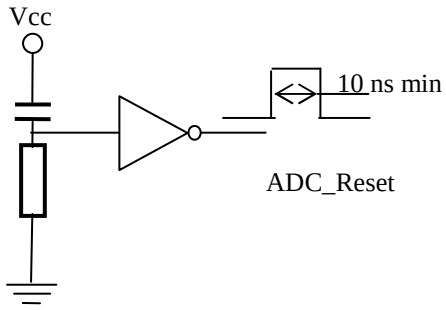


6.1.3 Slow control AGET task T6.2

Sc_ck = AGET_Sclk
Sc_en = SC_AGET
IF R/W= 0
    Sc_din = HZ
    Sc_dou = AGET_DIO
Else
    AGET_DIO=Sc_din
    Sc_dou = HZ
End if

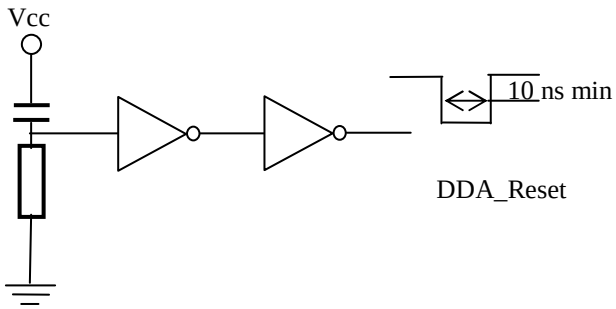
6.1.4 Slow control ADC task T6.3

SClk = ADC_Sclk
SEn = SC_ADC
SData = ADC_Data



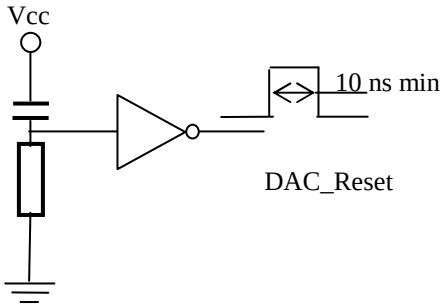
6.1.5 Slow control DDA task T6.4

DDA_Clk = DDA_Sclk
S_to_par_dat = DDA_Data
DDA_En = SC_DDA



6.1.6 Slow control DAC task T6.5

Sc_dac_clk = DAC_Sclk
Sc_dac_cs = SC_SC_DAC
DAC_DIO = Sc_dac-dio



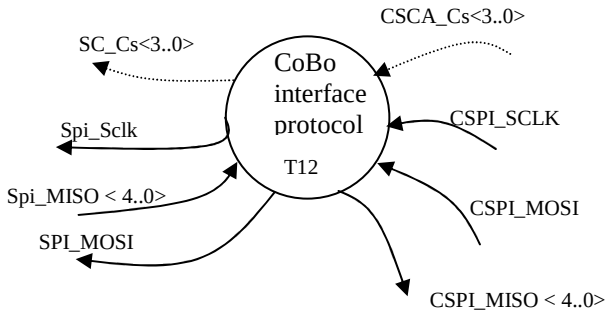
6.1.7 Slow control ID task T6.6

(c.f. task 8)

Chapter 7

CoBo Interface protocol Task T12

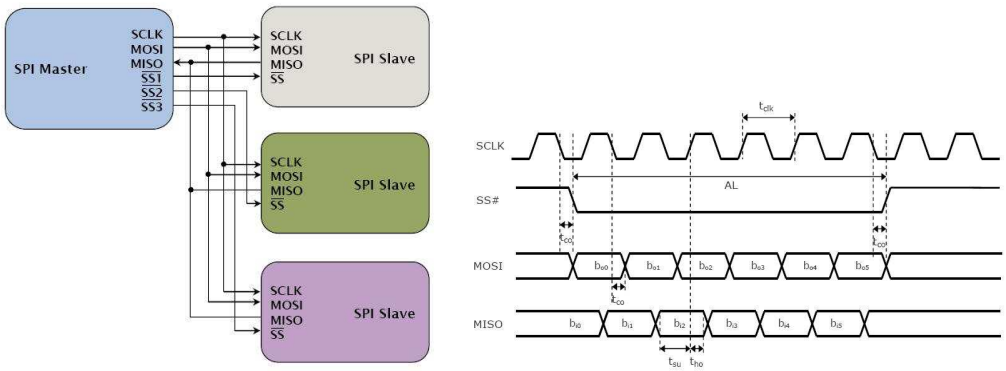
7.1 Task description



This task implements the SPI Bus , in SLAVE MODE.
The Serial Peripheral Interface Bus or SPI is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slaves can be connected to a single Master and the 'classical' SPI standard is defined as a 4-wires interface including:

- SCLK - a clock signal generated by the master;
- MOSI - (Master Out Slave In) a master-to-slave(s) serial line;
- MISO – (Master In Slave Out) a slave(s)-to-master serial line;
- SS# - one or several slave select lines.

CSPI_MISO < 4..0> : ASIC serial data out <3..0> AND DAC <4> out.



Symbol	Parameter	Min	Max	Units
t_{clk}	Clock period	20	1,250,000	ns
t_{co}	Clock to output	0	4	ns
t_{su}	Setup time	5.6	-	ns
t_{ho}	Hold time	-	0.0	ns
AL	Access length	1	32,000	bits

AsAd can be connected to a PC via a USB port for the test.

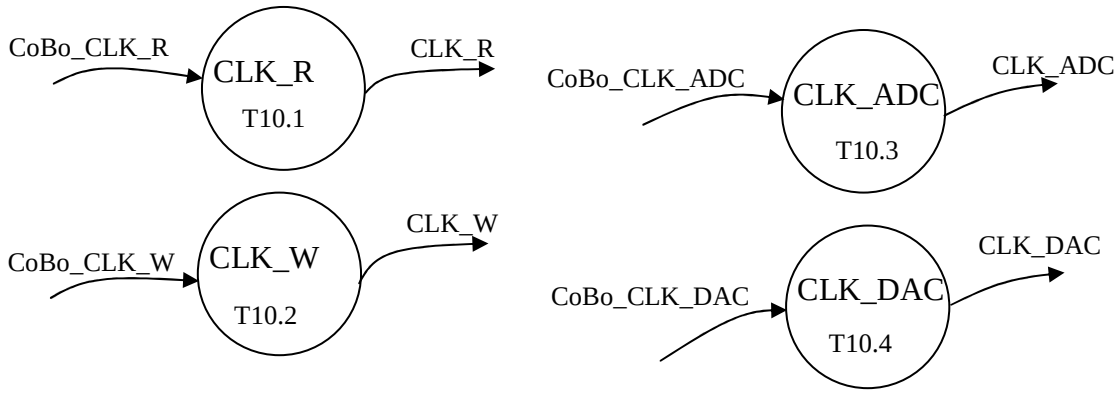
7.2 Technical part

Connector type and signal levels not yet defined

Chapter 8

Clock Distribution task T10

8.1 Task description



This task describes the distribution of clocks for writing and reading the SCA AGET.

8.2 Technical part

8.2.1 CLK_R and CLK_W

To ensure a good synchronization between all the system parts requiring CLK_R and CLK_W the use of low skew differential to LVDS fan-out buffers is suggested.

- Ics8543 (Integrated Circuit Systems, Inc).
  - 4 differential LVDS outputs
  - Tri-state
  - Selectable differential CLK, nCLK or LVPECL clock inputs
  - CLK, nCLK pair can accept the following differential
    - input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
  - PCLK, nPCLK supports the following input types:
    - LVPECL, CML, SSTL
- Maximum output frequency: 800MHz

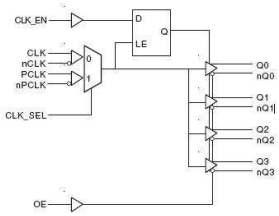


TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				800	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 800MHz	1.7		2.6	ns
*t*sk(o)	Output Skew; NOTE 2, 4				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	150		350	ps
t_F	Output Fall Time	20% to 80% @ 50MHz	150		350	ps
odc	Output Duty Cycle		45	50	55	%

All parameters measured at 500MHz.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

8.2.2 CLK_ADC

AD conversion requires an input clock that initiates the process at its first rising edge, on all enabled channels simultaneously. This signal should match with LVPECL levels. Receiver/transmitter possible : MC100LVEP16-D (LVPECL)

The 100 Series contains temperature compensation.

Features

- 240 ps Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.8 V
- V_{BB} Output
- Open Input Default State
- LVDS Input Compatible
- Pb−Free Packages are Available

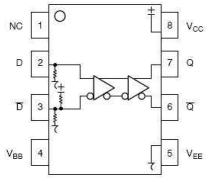


Table 5. 10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	17	22	27	17	22	27	17	22	28	mA
V_{OH}	Output HIGH Voltage (Note 8)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 8)	1365	1540	1665	1430	1605	1730	1490	1665	1790	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single Ended)	1365		1690	1430		1755	1490		1815	mV
V_{BB}	Output Voltage Reference (Note 9)	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D D̄	0.5 −150			0.5 −150			0.5 −150			μA

Table 10. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.8 V to −2.375 V or V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V (Note 27)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2. F_{max}/JITTER)		> 4			> 4			> 4		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	150	220	300	170	240	320	190	260	330	ps
t_{SKEW}	Duty Cycle Skew (Note 28)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	CLOCK Random Jitter (RMS) @ ≤ 1.0 GHz @ ≤ 1.5 GHz @ ≤ 2.0 GHz @ ≤ 2.5 GHz @ ≤ 3.0 GHz @ ≤ 3.5 GHz		 0.134 0.077 0.115 0.117 0.122 0.123	 0.2 0.2 0.2 0.2 0.2 0.2		 0.147 0.104 0.141 0.132 0.143 0.145	 0.3 0.3 0.3 0.3 0.3 0.3		 0.166 0.145 0.153 0.156 0.177 0.202	 0.3 0.3 0.3 0.3 0.3 0.3	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% − 80%) Q, Q̄	70	120	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

27. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
28. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

8.2.3 CLK_DAC

DA conversion requires an input clock that initiates the process at its first rising edge.This signal should match with LVPECL levels. We can use the buffer than CLK_ADC.

Chapter 9

ASAD monitoring task T9

Introduction

ASAD board is able to monitor the temperature at which it is operated, its power supply voltage levels and its power consumption.
All these measurements can be obtained from the referenced ADT7519 device, the following task description is thus based on this device capabilities.

9.1 Task description

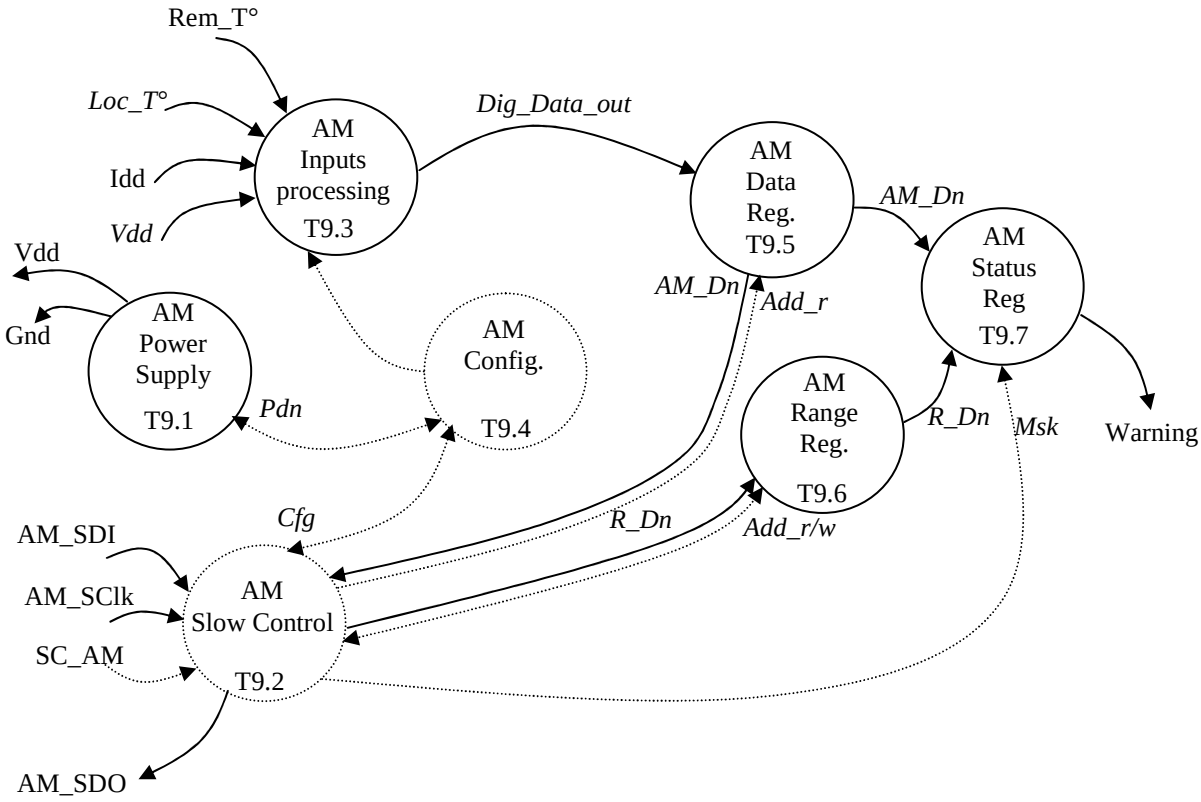


Figure 9.1: ASAD monitoring (Mainly based on ADT7519 datasheet)

Task T9.1

ASAD monitoring (AM) requires a single 0V-3.3V power supply. Typical power consumption for this supply is given at 10mW.

Task T9.2

AM settings are tuned by means of a SPI slow control interface that deals with four signals called AM_SDI (Serial Data Input), AM_SDO (Serial Data Output), AM_SClk (Serial Clock 20MHz max), and SC_AM (Chip Select).
This transfer protocol has to be selected **50ms** (device settling time) after the device power up, by sending down 3 SC_AM pulses (figure 9.2).

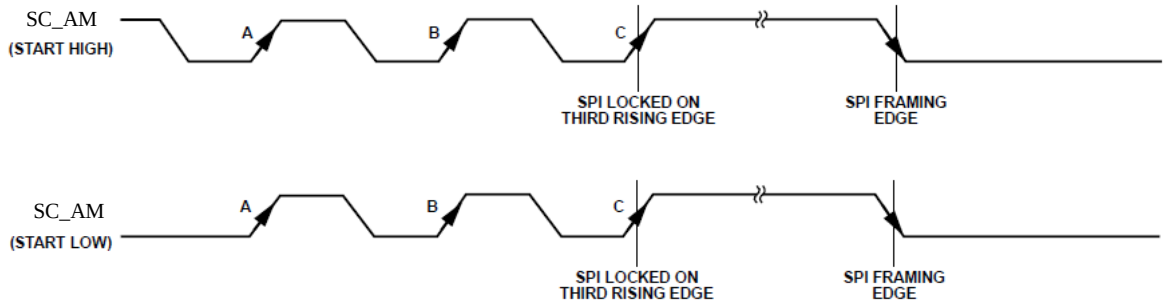


Figure 9.2: SPI transfer protocol selection and locking (Extracted from the ADT7519 datasheet)

Various 8-bit registers can thus be accessed to perform ASAD monitoring.
This is achieved by setting low SC_AM and by sending a command through AM_SDI which is synchronous with AM_SClk. The command contains at first an instruction byte which indicates a write (x90) or a read (x91) operation.
To write into a register, the first instruction byte (x90) is at least followed by two other bytes:

- an address byte which is stored into a pointer register
- a data byte which is written at the address defined by the pointer register

More than one data byte can be send. In this case, subsequent data bytes are written into sequential writable registers, as the pointer register auto-increments from the first address specified.
The writing sequence is illustrated in figure 9.3

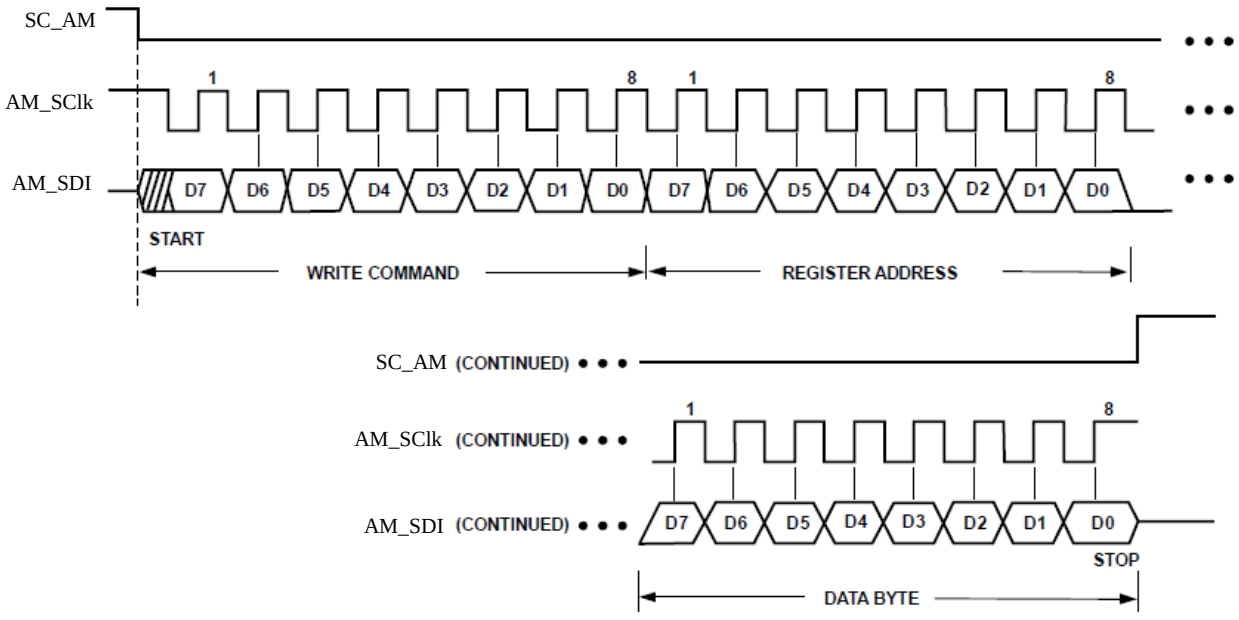


Figure 9.3: SPI writing to the pointer register diagram followed by a single byte of data to write in the selected register (Extracted from the ADT7519 datasheet)

To read from one register, the first operation consists in writing into the pointer register its address. Then a read command (0x91) is send through AM_SDI and the data are readout trough AM_SDO (sequentially according to the auto-incremented address contained in the pointer register until SC_AM goes high as stated in figure 9.4.2)

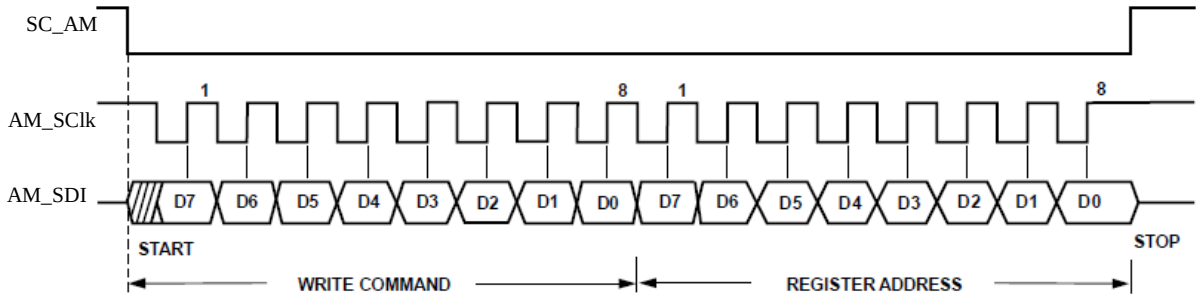


Figure 9.4.1: Writing to the pointer register to select a register for subsequent read operation (Extracted from the ADT7519 datasheet)

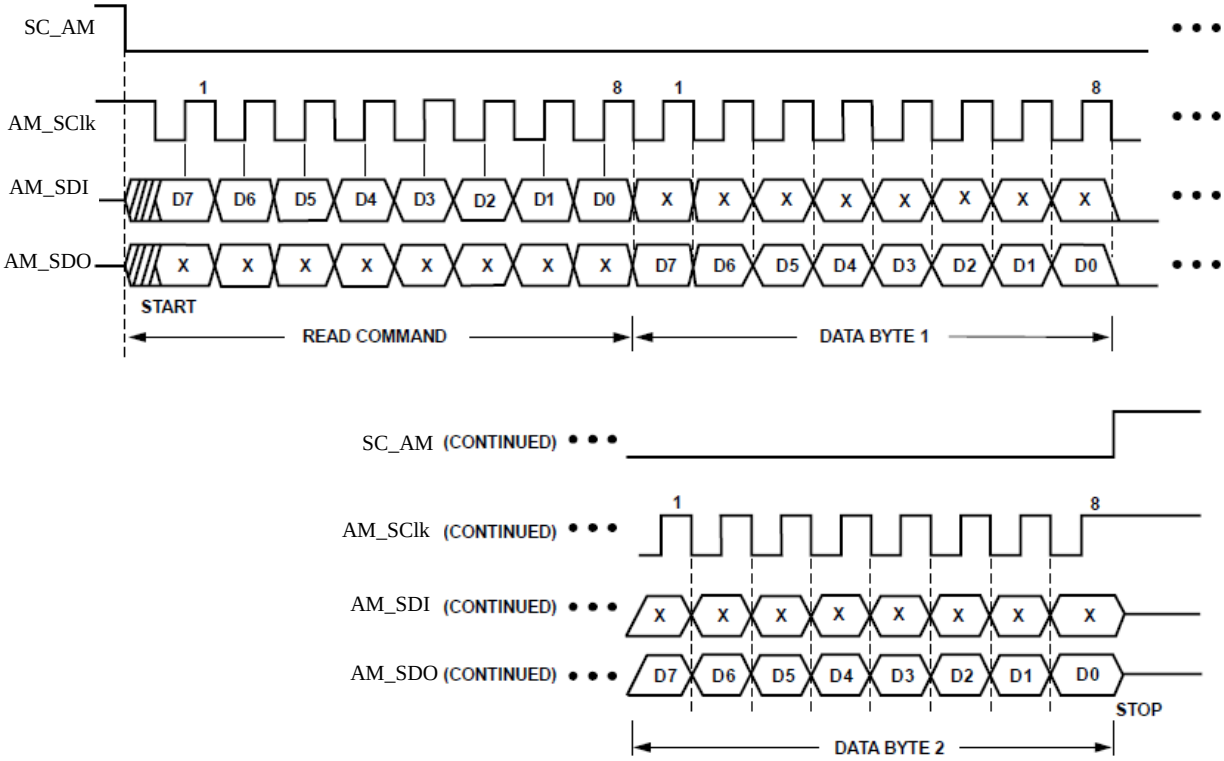


Figure 9.4.2: Reading two bytes of data from two sequential registers (Extracted from the ADT7519 datasheet)

Figure 9.4: SPI reading process

Task T9.3

AM inputs are voltages and physical quantities proportional to voltages (Vdd is the power supply voltage, Idd is the power supply current inferred from a voltage drop across a resistive

load, Loc_T° and Rem_T° are two temperatures given by the voltage drop across a semi-conductor junction).
As shown in figure 9.5 (task T9.3.1), these voltages are applied at the inputs of an analogue multiplexor which drives out the one that is digitized by the 10-bit ADC involved in task T9.3.2. The voltage selected to be digitized is defined by the configuration mode set in Task 9.4 section. The ADC full scale reference in use can be whether the power supply voltage Vdd or an internal voltage given by a band gap voltage reference (task T.3.3). This selection (*Ref_sel*) is operated in Task 9.4 section, as well as the selection of the conversion rate (*Frq_sel*) which is given by an internal clock (*ck*) running at whether 1.4 kHz or 22kHz

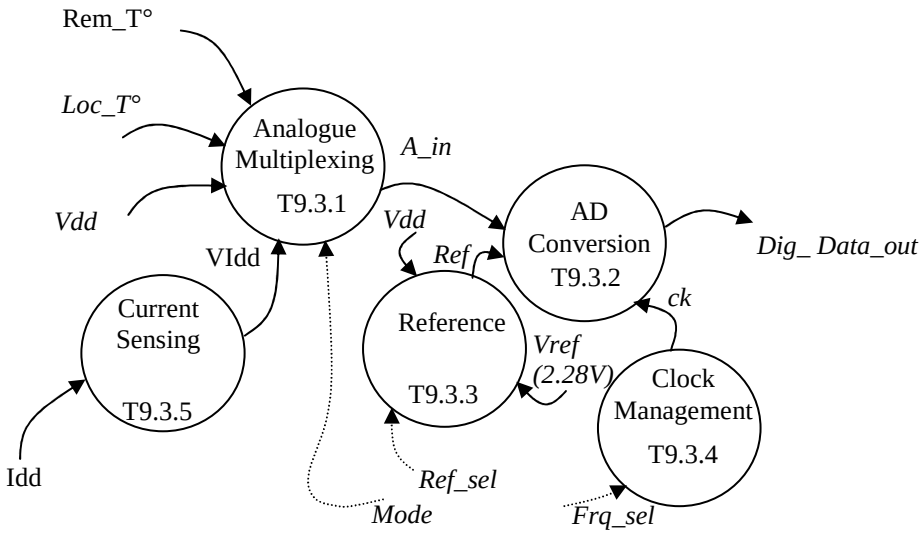


Figure 9.5: AM inputs processing (Task T9.3 details)

Dig_data_out is the code value extracted from the 10-bit successive approximation AD converter. This code format depends on the selected input to be converted:

- In case of supply voltage (Vdd) monitoring

The code corresponds with the natural binary value of the supply voltage divided by the product of the ADC LSB and a well known scale factor. The scale factor (3.07) corresponds with the device maximum supply voltage (7V) divided by the reference value (*Vref*=2.28V). The ADC LSB is the reference value (2.28V) divided by 1024, (equal to 2.226 mV). The code for the nominal supply voltage (3.3V) is then 01 1110 0010 in natural binary (or 1E2 in hexadecimal)

- Case of temperature monitoring

There is two temperature sensors which enable to make a local temperature measurement (Loc_T°) and a remote temperature measurement (Rem_T°). In both case semi-conductor junctions are used as sensors. The two junctions are biased with two currents I and N.I (figure 9.6). The difference between the voltages drops across the two junctions (ΔV_{BE}) is proportional to the temperature:
$T° = (\Delta V_{BE}.q.\ln N)/ k$ (q is the elementary charge, k is Boltzmann's constant)

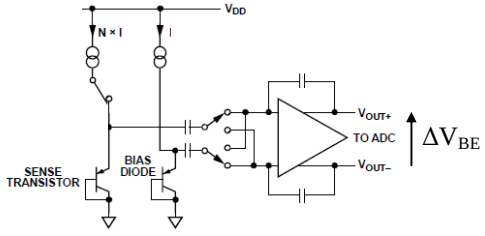


Figure 9.6: Temperature measurements (Extracted from the ADT7519 datasheet)

As temperature can vary from -40°C to 128°C in default configuration, the ΔV_{BE} voltage can be either positive or negative and the corresponding coded value extracted from the ADC is given in a twos complement format as shown in figure 9.7

Temperature Data Format
(Internal and External Temperature)

Temperature	Digital Output
–40°C	11 0110 0000
–25°C	11 1001 1100
–10°C	11 1101 1000
–0.25°C	11 1111 1111
0°C	00 0000 0000
+0.25°C	00 0000 0001
+10°C	00 0010 1000
+25°C	00 0110 0100
+50°C	00 1100 1000
+75°C	01 0010 1100
+100°C	01 1001 0000
+105°C	01 1010 0100
+125°C	01 1111 0100

Figure 9.7: Temperature data format (Extracted from the ADT7519 datasheet)

A calibration should be made before the temperature measurement by using the same biasing current I for the two junctions. Thus the same voltage drop should appear across the two junctions and ΔV_{BE} should be zero. In case of non-zero value the data coded is stored into an offset register and is used as compensation.

Figures 9.8 and 9.9, show the complete circuits in use for respectively local and remote temperature measurements.

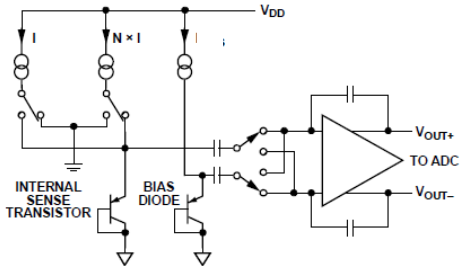


Figure 9.8: Structure of internal temperature sensor (Extracted from the ADT7519 datasheet)

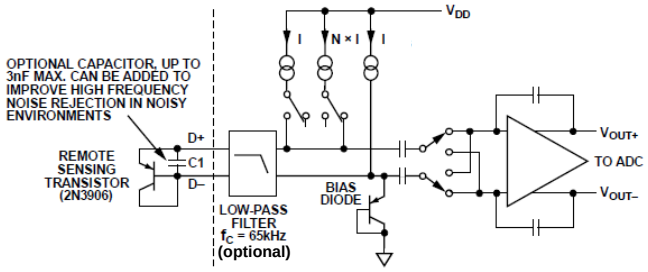


Figure 9.9: Structure of external temperature sensor (Extracted from the ADT7519 datasheet)

- Case of supply current monitoring

Output code format is given in natural binary.
The measured value depends on the signal conditioning made in task 9.3.5
A detailed diagram of the structure used to perform the task 9.3.5 is given in figure 9.10

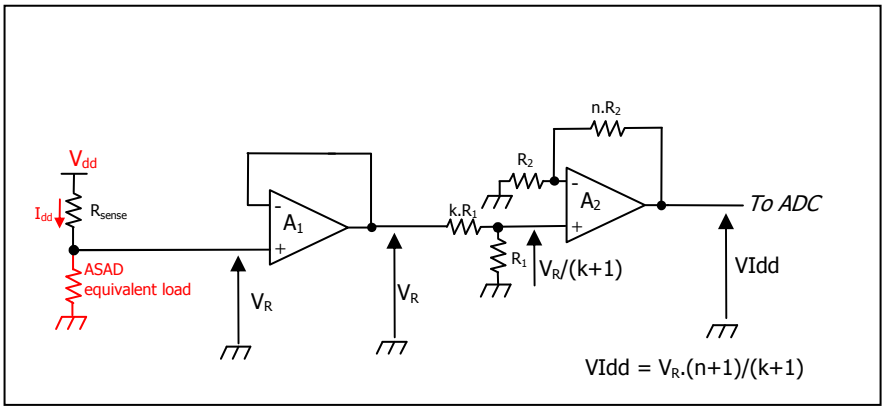


Figure 9.10: Structure used to perform task 9.3.5

According to figure 9.10:
The current Idd trough the resistor R_{sense} establishes the voltage $V_R = Vdd - Idd.R_{sense}$.
So the voltage VIdd applied at the ADC input is given by:
$VIdd = (Vdd - Idd.R_{sense}).(n+1)/(k+1)$
As Vdd can be monitored, R_{sense}, n and k are known parameters, measuring VIdd enables to monitor Idd.
Assuming 7.92W maximal power consumption for ASAD with a Vdd voltage equal to 3.3V gives Idd_{max}=2.4A
R_{sense} for example equal to 0.01Ω implies a voltage drop across Rsense equal to 24mV. V_R is then equal to 3.276V. Setting n=1 and k=2 gives VIdd=2.184V. Using the 2.28V ADC reference, the equivalent output code is 11 1101 0100 in natural binary (or 3D4 in hexadecimal)

Task T9.4

AsAd Monitoring configuration is made by means of the SPI interface (c.f. Task T9.2)
Three 8-bit Control Configuration Registers (CCR) can be accessed in read or write operation.
Each CCR contains by default a byte of zeros at power up.

- The 1st CCR is accessible at the address x18 and is filled as shown in figure 9.11

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	1

Figure 9.11: 1st Control Configuration Register content

D7 at 1 would power down AsAd monitoring devices it is then kept at 0
D6 at 1 configures the warning signal (see figure 9.1 and Task 9.7) to be active high
D5 at 0 enables to emit a warning signal whenVdd, Loc_T°,Rem_T° or VIdd, are out of range
D4 at 0 is reserved
D3 at 1 enables to use the analogue multiplexor (c.f. fig. 9.5) 3rd physical input
D2 at 0 and D1 at 1 enable the external temperature sensing (D+ & D- shown in fig 9.9 are the 1st and 2nd physical inputs)
D0 at 1 enables the monitoring (by default in round robin mode*).
*The round robin mode corresponds with a cycle in which are sequentially taken measurements of Vdd, Loc_T°, Rem_T° and VIdd. Once all conversions are completed by the ADC, the monitoring device loops around for another measurement cycle.

- The 2nd CCR is accessible at the address x19 and is filled as shown in figure 9.12

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	x	x	x

Figure 9.12: 2nd Control Configuration Register content

D7 at 1 would be equivalent to a software reset it is then kept at 0 by default
D6 is kept at 0 when using a SPI transfer protocol
D5 at 0 enables to average Vdd, Loc_T°, Rem_T° and VIdd values over 16 measurements
D4 at 0 enables round robin mode. Setting it at 1 enables to take only one channel measurement which is defined by the D0, D1, D2 values (*Mode* in figure 9.5)
D3 at 0 is reserved

If D4 at 1 and:

[D0:D2]=000 only Vdd can be monitored
[D0:D2]=001 only Loc_T° can be monitored
[D0:D2]=010 only Rem_T° can be monitored
[D0:D2]=100 only VIdd can be monitored

- The 3rd CCR is accessible at the address x1A and is filled as shown in figure 9.13

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Figure 9.13: 3rd Control Configuration Register content

D7 at 0 is reserved
D6 is kept at 0 as this bit is not in use in AsAd monitoring
D5 is kept at 0 as this bit is not in use in AsAd monitoring
D4 at 0 enables to use internal Vref as the reference for the ADC (*Ref_sel* in figure 9.5)
D3 is kept at 0 as this bit is not in use in AsAd monitoring
D2 at 0 is reserved
D1 is kept at 0 as this bit is not in use in AsAd monitoring
D0 at 0 sets the ADC clock at 1.4 kHz (*Frq_sel* in figure 9.5) and enables the active filter shown in figure 9.9

Task T9.5

AsAd Monitoring can be achieved by reading (*Add_R*) the values (*AM_Dn*) stored in AM Data Registers

- Vdd, 10-bit value [B0:B9], is available by reading Vdd Value Register MSB at the address x06 and Vdd Value Register LSB at the address x03
  The bit map is given in figure 9.14

Vdd Value Register MSB (Address =* x06*)

D7	D6	D5	D4	D3	D2	D1	D0
B9	B8	B7	B6	B5	B4	B3	B2

Vdd Value Register LSB (Address =* x03*)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	B1	B0	-	-

Figure 9.14: Monitoring the Vdd value

- Loc_T°, 10-bit value in twos complement format [B0:B9], is available by reading Int. Temp. Value Register MSB at the address x07 and Int. Temp Value Register LSB at the address x03
  The bit map is given in figure 9.15

Int. Temp. Value Register MSB (Address = x07)

D7	D6	D5	D4	D3	D2	D1	D0
B9	B8	B7	B6	B5	B4	B3	B2

Int. Temp. Value Register LSB (Address = x03)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	B1	B0

Figure 9.15: Monitoring the Loc_T° value

- Rem_T°, 10-bit value in twos complement format [B0:B9], is available by reading Ext. Temp. Value Register MSB at the address x08 and Ext. Temp Value Register LSB at the address x04
  The bit map is given in figure 9.16

Ext. Temp. Value Register MSB (Address = x08)

D7	D6	D5	D4	D3	D2	D1	D0
B9	B8	B7	B6	B5	B4	B3	B2

Ext. Temp. Value Register LSB (Address = x04)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	-	B1	B0

Figure 9.16: Monitoring the Rem_T° value

- VIdd, 10-bit value [B0:B9], is available by reading VIdd Value Register MSB at the address x0A and VIdd Value Register LSB at the address x04
  The bit map is given in figure 9.17

VIdd Value Register MSB (Address = x0A)

D7	D6	D5	D4	D3	D2	D1	D0
B9	B8	B7	B6	B5	B4	B3	B2

VIdd Value Register LSB (Address = x04)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	B1	B0	-	-	-	-

Figure 9.17: Monitoring the VIdd value

Task T9.6

AsAd Monitoring enables to define the acceptable range within which a measured value can vary. Such control is made possible by setting the upper and lower limits *(R_Dn)* of the ranges. Eight 8-bit read/write register are devoted to this task:

Vdd High Limit Register (Address = x23)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	1	1	1

Figure 9.18: Default value in Vdd High Limit Register (natural binary code for 5.46V)

Vdd Low Limit Register (Address = x24)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	1	0

Figure 9.19: Default value in Vdd Low Limit Register (natural binary code for 2.7V)

Int. Temp. High Limit Register (Address = x25)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	1	0	0

Figure 9.20: Default value in Int. Temp. High Limit Register (twos complement code for 100°C)

Int. Temp. Low Limit Register (Address = x26)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	1	0	0	1

Figure 9.21: Default value in Int. Temp. Low Limit Register (twos complement code for -55°C)

Ext. Temp. High Limit Register (Address = x27)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Figure 9.22: Default value in Ext. Temp. High Limit Register (twos complement code for -1°C)

Ext. Temp. Low Limit Register (Address = x28)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Figure 9.23: Default value in Ext. Temp. Low Limit Register (twos complement code for 0°C)

VIdd High Limit Register (Address = x2D)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Figure 9.24: Default value in VIdd High Limit Register (natural binary code for 2.28V)

VIdd Low Limit Register (Address = x2E)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

Figure 9.25: Default value in VIdd Low Limit Register (natural binary code for 0V)

Task T9.7

AsAd Monitoring device is able to generate its own warning signal (c.f. Task 9.4, 1st CCR) as soon as a value stored in the AM data register (c.f. Task 9.5) is found:

- greater than its high limit defined in Task 9.6
- less than or equal to its low limit defined in Task 9.6

Once a warning signal has been emitted, two 8-bit status registers (read only) can be accessed to find the parameter that is out of bound.

In the 1st status register (address x00),

- Bit D6 value is 1 if VIdd is out of bound
- Bit D4 value is 1 if a fault of the remote temperature sensor is detected (open or short)
- Bit D3 value is 1 if Rem_T° is below the low limit set in Task 9.6
- Bit D2 value is 1 if Rem_T° exceeds the high limit set in Task 9.6
- Bit D1 value is 1 if Loc_T° is below the low limit set in Task 9.6
- Bit D0 value is 1 if Loc_T° exceeds the high limit set in Task 9.6

In the 2nd status register (address x01),

- Bit D4 value is 1 if Vdd is out of bound

A read operation of these registers resets their contents provided that the warning origin has been corrected.

The fault detection on any inspected parameter can be enabled or disabled using two 8-bit mask registers (accessible for read or write operations)
In the 1st mask register (address x1D),

- Bit D7 value has to be 1
- Bit D6 at 1 disables a warning caused by an out of bound detected on VIdd value
- Bit D5 value has to be 1
- Bit D4 at 1 disables a warning caused by a fault detected on the remote temp. sensor
- Bit D3 at 1 disables a warning caused by Rem_T° below its low limit
- Bit D2 at 1 disables a warning caused by Rem_T° over its high limit
- Bit D1 at 1 disables a warning caused by Loc_T° below its low limit
- Bit D0 at 1 disables a warning caused by Loc_T° over its high limit

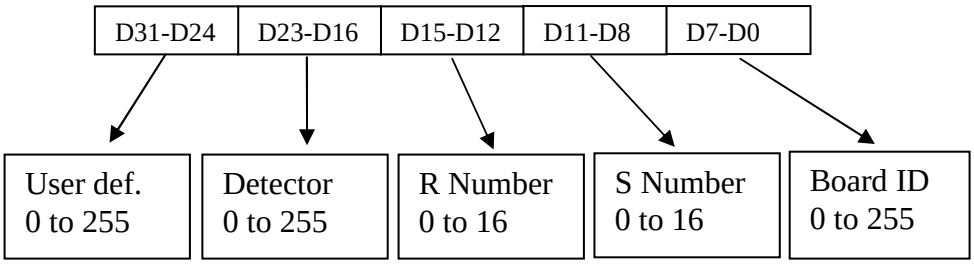
In the 2nd mask register (address x1E), all bits are reserved except D4. Bit D4 at 1 disables a warning caused by an out of bound detected on Vdd value

Chapter 10

Identification task T8

10.1 Task description

AsAd identifier in the whole GET system



Chapter 11

AsAd Power Supply Task T11

Introduction

AsAd board generates its own 3.3V power supply voltage (Vdd) from the GET power supply unit.
A power consumption summary allows evaluating an approximation of the current supply Idd required:

Task to be carried out	Involved device	Devices qty/AsaD	Power/ device (mW)	Power/ AsAd (mW)
T1	AGET	4	720 (max)	2900
T2	ADC ADS6422	1	1250 (max)	1250
T4	LVDS receivers SN65LVDS348	1	70 (max)	70
T5	DAC AD9707	1	60 (max)	60
T6	CPLD XC95288XL	1	280 (typ)	280
T8	LVDS fanout buffers ICS8543	2	160 (max)	320
T8	LVPECL buffers MC100LVEP16	2	120 (max)	240
T9	ADT 7519	1	10 (max)	10
	All devices			5130
	Safety margin	1	20 % total 1040	1040
	TOTAL			**6170**

The 3.3V Vdd should thus supply an approximate 1.9A Idd current (6.27W)
In order to minimize energy losses, a low-dropout (LDO) regulator able to supply the current required has to be implemented. The ultra-LDO TPS74401 is a well suited device; the following task description is thus based on this device capabilities.

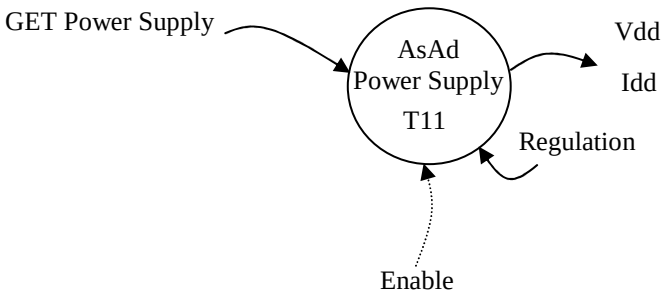


Figure 11.1: AsAd power supply Task T11

The regulator output can be tuned at 3.3V with 1% accuracy over load, line and temperature and is able to supply a 3A current. An internal current limit allows protecting the device when the output current reaches 3.5A and a thermal protection ensures to disable the output when the temperature reaches 155°C, until the device is cooled enough.
The output voltage regulation is independent from the power source as shown in figure 11.2 allowing thus to minimize energy loss. To generate a 3.3V output Vdd, the power source voltage can be as low as 3.5V (for a 2A Idd the power loss is only 600mW). On the other hand, a V_{BIAS} voltage at least equal to Vdd voltage plus 1.62V is required to make the device work properly (A 5V voltage able to supply 4mA is enough).

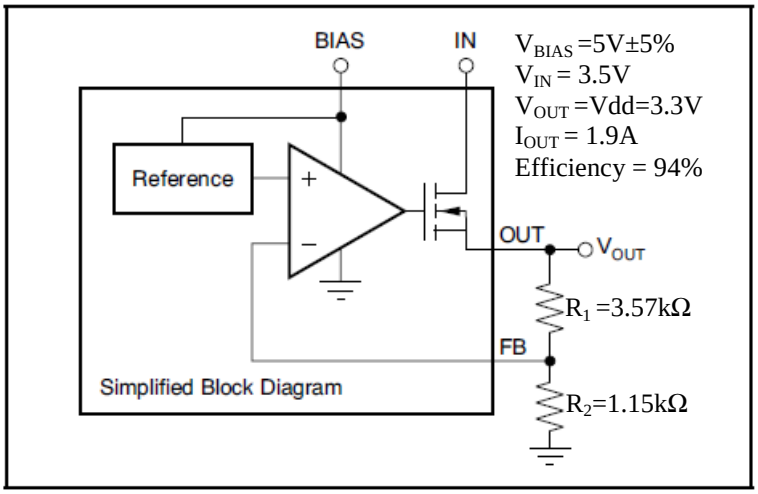


Figure 11.1: Vdd generator structure (extracted from TPS74401 datasheet)

R1 in the feedback loop together with R2 establishes Vdd= $0.8V \times \left(1 + \frac{R_1}{R_2}\right)$

V_{BIAS} voltage can be obtained from a MAX 756 (circuit connections are shown in figure 11.2)

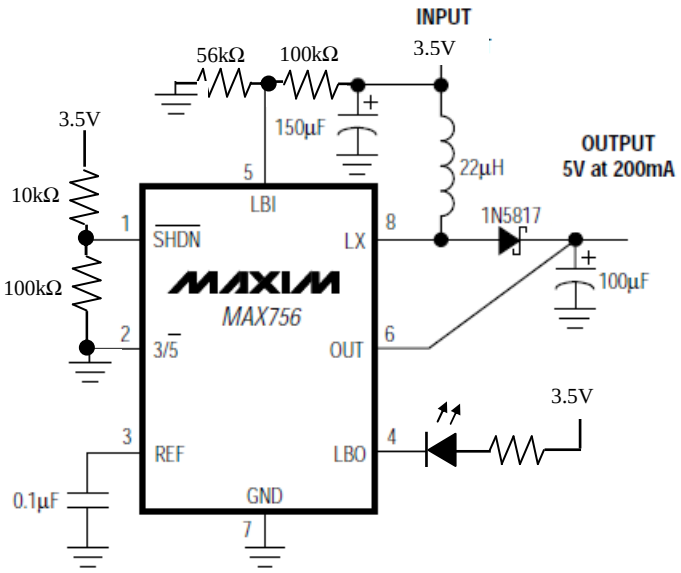


Figure 11.2: Vbias generator structure (extracted from MAX756 datasheet)

The 10kΩ/100kΩ voltage divider enables the 5V output voltage obtained from the 3.5V power supply
The 100kΩ/56kΩ voltage divider checks for the 3.5V presence.
If the power supply voltage is lower than 3.5V, the LED is lit on

When V_{BIAS} and V_{IN} (3.5V from GET power supply unit) are correctly applied to the TPS74401 LDO, a 3.3V "enable" signal has to be sent from the slow control in order to supply AsAd (as long as this signal level is 0V, AsAd supply is switched off).

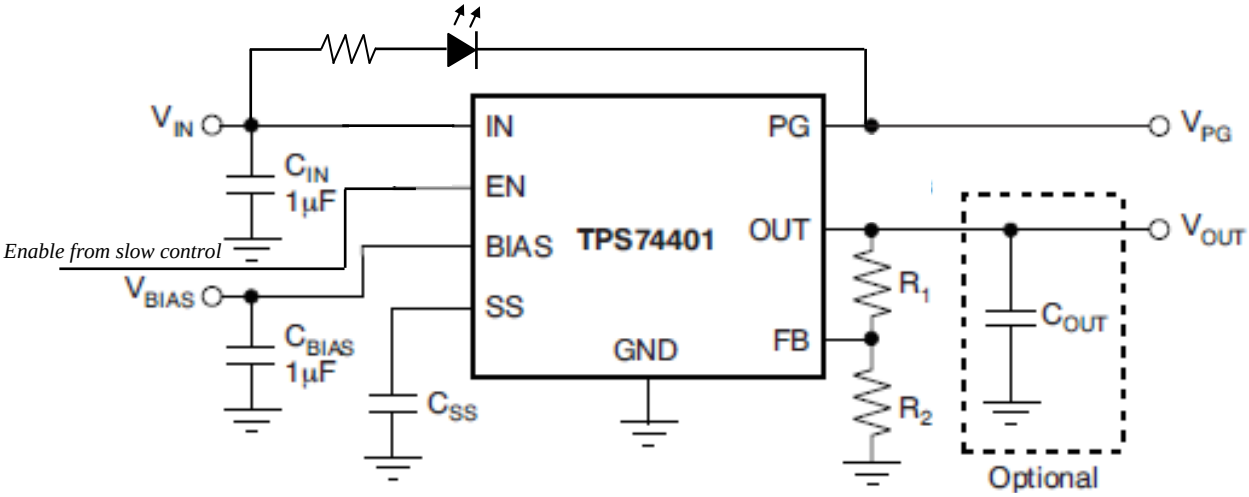


Figure 11.3: TPS74401 external connections (extracted from TPS74401 datasheet)

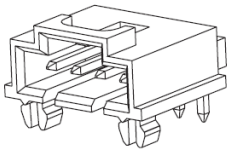
The LED shown in figure 11.3 is lit on as long as Vout is kept below 90% of Vdd.
The settling time required to reach a 3.3V Vdd value mostly depends on the C_{OUT} value. This capacitor, that represents the sum of all by-passing capacitances in AsAd, can take any value without affecting the Vdd stability. If C_{OUT} value is less than C_{SS} value, Vdd settling time is given by $ts = \frac{0.8 \times C_{ss}}{730.10^{-9}}$

The connection between GET power supply and AsAd has to be point to point in order to use high density connectors. These connectors have to bear a 3A maximal current and must have a low resistive feature (gold plated connections are best suited).
The Molex 70551 series which have good mechanical properties (figure 11.4) can be used for AsAd.

2.54mm (.100") Pitch SL™ Wire-to-Board Shrouded Header

70551

Single Row, .120" Pocket Right Angle, Split Peg



Features and Benefits
- Sizes 2 to 25 circuits
- PCB locks hold header in place until permanently soldered
- Locking crown secures positive latch connector to header
- Polarization slots guide front ribs of mating connector to prevent pin damage
- Standoffs minimize flux retention

Reference Information
Product Specification: PS-70541
Packaging: Tube
UL File No.: E29179
CSA File No.: LR19980
Mates with: 70066, 70066N, 70400 and 70430G
Designed in: Inches

Electrical
Voltage: 250V
Current: 3.0A
Contact Resistance: 15 milliohms max.
Dielectric Withstanding Voltage: 1500V
Insulation Resistance: 10,000 Megohms min.

Mechanical
Insertion force to PCB: 44.48N (10 lbs.)
Durability: Tin — 25 cycles; Gold — 50 cycles

Physical
Housing: Black polyester, UL 94V-0
Contact: Copper Alloy
Plating: See Table
Operating Temperature: -40 to +105˚C

Circuits	Order No.			Lead-free
	150µ" Tin	15µ" Gold	30µ" Gold	
2	70551-0001	70551-0036	70551-0071	Yes
3	70551-0002	70551-0037	70551-0072	
4	70551-0003	70551-0038	70551-0073	
5	70551-0004	70551-0039	70551-0074	
6	70551-0005	70551-0040	70551-0075	
7	70551-0006	70551-0041	70551-0076	
8	70551-0007	70551-0042	70551-0077	
9	70551-0008	70551-0043	70551-0078	
10	70551-0009	70551-0044	70551-0079	
11	70551-0010	70551-0045	70551-0080	
12	70551-0011	70551-0046	70551-0081	
13	70551-0012	70551-0047	70551-0082	

Circuits	Order No.			Lead-free
	150µ" Tin	15µ" Gold	30µ" Gold	
14	70551-0013	70551-0048	70551-0083	Yes
15	70551-0014	70551-0049	70551-0084	
16	70551-0015	70551-0050	70551-0085	
17	70551-0016	70551-0051	70551-0086	
18	70551-0017	70551-0052	70551-0087	
19	70551-0018	70551-0053	70551-0088	
20	70551-0019	70551-0054	70551-0089	
21	70551-0020	70551-0055	70551-0090	
22	70551-0021	70551-0056	70551-0091	
23	70551-0022	70551-0057	70551-0092	
24	70551-0023	70551-0058	70551-0093	
25	70551-0024	70551-0059	70551-0094	

Figure 11.4: Power supply connector (extracted from Molex datasheet)