## T2K TPC Read-out Electronics

## Digital Front-end Mezzanine Card Design Notes

- I. Introduction (p.1)
  - 1. Scope
  - 2. Brief online of the TPC readout architecture
- II. Reduced FEM cards (p.2)
  - 1. Concept
  - 2. Variations (p.3)
  - 3. Development plan
- III. FEM card on-board components (p.4)
  - 1. FPGA target (p.5)
    - 1.1 Vendor and family
    - 1.1 Part number, package and speed grade
  - 2. FPGA configuration (p.6)
    - 2.1 Principle
    - 2.1 Configuration PROM and protocol
    - 2.1 JTAG chains (p.7)
  - 3. Front-end card ADC (p.8)
  - 4. Buffer memory (p.8)
    - 4.1 Speed and size requirement
    - 4.1 Technology options and discussion
  - 5. Optical transceiver (p.10)
  - 6. Local oscillator (p.11)
  - 7. Board identification (p.11)
  - 8. Voltage, current and temperature monitoring (p.12)
  - 9. Slow control and monitoring
    - 9.1 Justification of need (p.12)
    - 9.1 Items to control and monitor (p.13)
    - 9.1 Micro controller choice and slow control protocol (p.13)
    - 9.1 Micro controller digital IP port usage (p.14)
    - 9.1 Micro controller embedded ADC (p.16)
    - 9.1 Micro controller power on reset and clock (p.16)
    - 9.1 Slow control CANbus Interface (p.17)
    - 9.1 Slow control MSCB interface (p.18)
    - 9.1 Slow control network connectors and physical layer (p.19)
  - 10. On-board power supplies (p.20)
    - 10.1 Power-on configuration and reset (p.24)
    - 10.1 FPGA IO bank voltage and decoupling (p.25)
  - 11. Debug and expansions I/Os (p.27)
    - 11.1 Expansion RS-232 terminal (p.27)

- 11.1 Extension cable (p.28)
- 11.1 Debug pins and expansion slot (p.29)
- 12. Variations for reduced FEM cards (p.30)
- IV. Interface to Analog Front-end cards
  - 1. Principles (p.31)
  - 2. List of FEM/FEC interface signals (p.31)
  - 3. Distribution of output signals and multiplexing of input signals (p.33)
    - 3.1 General control signals (p.33)
    - 3.1 SCA control signals (p.35)
    - 3.1 ADC signals (p.36)
    - 3.1 Test and configuration signals (p.36)
    - 3.1 Signals specific to the testbench of the ASIC (p.38)
    - 3.1 FEC, FEM and Micromegas detector identification chips (p.39)
    - 3.1 FEC presence detection (p.39)
- V. FEM physical design aspects
  - 1. Printed circuits board (p.39)
- VI. FEM Firmware
  - 1. Outline of the firmware (p.43)
  - 2. FEM resister map (p.44)
    - 2.1 Register 0x00 (p.45)
    - 2.1 Register 0x02 (p.46)
    - 2.1 Register 0x04 (p.46)
    - 2.1 Register 0x05 (p.46)
    - 2.1 Register 0x06 (p.46)
    - 2.1 Register 0x07 (p.47)
    - 2.1 Register 0x08 (p.47)
    - 2.1 Register 0x0A (p.48)
    - 2.1 Register 0x0C (p.48)
    - 2.1 Register 0x0D (p.48)
    - 2.1 Register 0x0E (p.48)
    - 2.1 Register 0x0F (p.48)
    - 2.1 Register 0x10 (p.49)
    - 2.1 Register 0x11 (p.49)
    - 2.1 Register 0x12 (p.49)
    - 2.1 Register 0x14 (p.49)
    - 2.1 Register 0x16 (p.50)
    - 2.1 Register 0x18 (p.50)
    - 2.1 Register 0x1A (p.50)
    - 2.1 Register 0x1C to 1F (p.52)

- 2.1 Register 0x20 to 0xFFF (p.52)
- 2.1 Register 0x1000 to 0x1FFF (p.52)
- 2.1 Address space from 0x2000 to 0x3FFF (p.52)
- 2.1 Address space from 0x4000 to 0x5FFF (p.53)
- 2.1 Address space from 0x6000 to 0xFFFF (p.53)
- 3. SCA data storage and retrieval in external buffer memory (p.53)
  - 3.1 Event data retrieval (p.56)
  - 3.1 Event data zero-supression (p.58)
  - 3.1 Event data pre-load via FEM registers (p.59)
- VII. Interface FEM card/ back-end Data Convertor Cards (p.61)
  - 1. Requirements (p.61)
  - 2. Principle (p.62)
  - 3. DCC to FEM link (p.63)
  - 4. FEM to DCC link (p.65)
    - 4.1 Slow control response packet (p.65)
    - 4.1 Event data fragment packet (p.66)
  - 5. DCC Implementation Challenges and Suggestions (p.67)
- VIII. Combined reduced FEM and DCC (p.68)
  - 1. Concept (p.68)
  - 2. Design tools and methodology (p.68)
  - 3. Reduced DCC and embedded processor system (p.68)
  - 4. Software (p.69)
    - 4.1 Libraries and test programs (p.70)
  - 5. Configuration of the FPGA evaluation kit (p.71)
  - 6. Embedded processor system functional test and performance (p.72)
    - 6.1 Processor bus level transfers (p.72)
    - 6.1 Remote FEM register access via the gigabit link (p.73)
    - 6.1 Functional test of the control of the pulser on-board the FEC (p.74)
    - 6.1 Read and write operations to FEC ASIC registers (p.77)
- IX. Reduced FEM test and SIC test bench (p.79)
  - 1. Hardware test (p.79)
  - 2. Interface connector to FEC/ASIC test board (p.79)
  - 3. Pulser DAC (p.80)
  - 4. Read and write operations to ASIC registers (p.81)
  - 5. Capturing ADC data (p.81)
  - 6. SCA write and read back phases (p.81)
    - 6.1 SCA data alignment (p.82)
    - 6.1 Retrieving the last read pointer in the SCA (p.83)
    - 6.1 Capturing the output of the internal pulser in the SCA (p.84)
    - 6.1 On-board voltage and temperature monitoring ADC (p.84)
    - 6.1 Data acquisition performance and limitations (p.85)
- X. Test of DCC to FEM clock/trigger distribution concept

- 1. Principle and test setup (p.87)
- 2. Clock forwarding with RocketIP transceivers (p.87)
- 3. Trigger and synchronous signals distribution with RocketIO transceivers (p.88)
- 4. SCA write clock generation and alignment (p.90)
- 5. Discussion (p.91)
- XI. Test of the prototype of the full size FEM (p.92)
  - 1. Board overview (p.92)
  - 2. Installation (p.92)
  - 3. Board power measurements (p.95)
  - 4. Verification of signals on FEC connectors (p.97)
  - 5. CAN bus slow control interface (p.99)
  - 6. Optical link performance (p.99)
  - 7. List of issues and modifications for the production model of the full size FEM (p.99)
    - 7.1 Hole missing on 80-pin connector JFEM2
    - 7.1 RJ45 connectors mis-oriented
    - 7.1 Trace width on slow control power lines is insufficient
    - 7.1 Nets LFE\_PR\_B<5..0> are not connected to any other net
    - 7.1 Geographical localization of boards at a global level is incomplete
- XII. References (p.100)